User's Guide
micro-line®
C44CPU

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1. General

1.1 Introduction

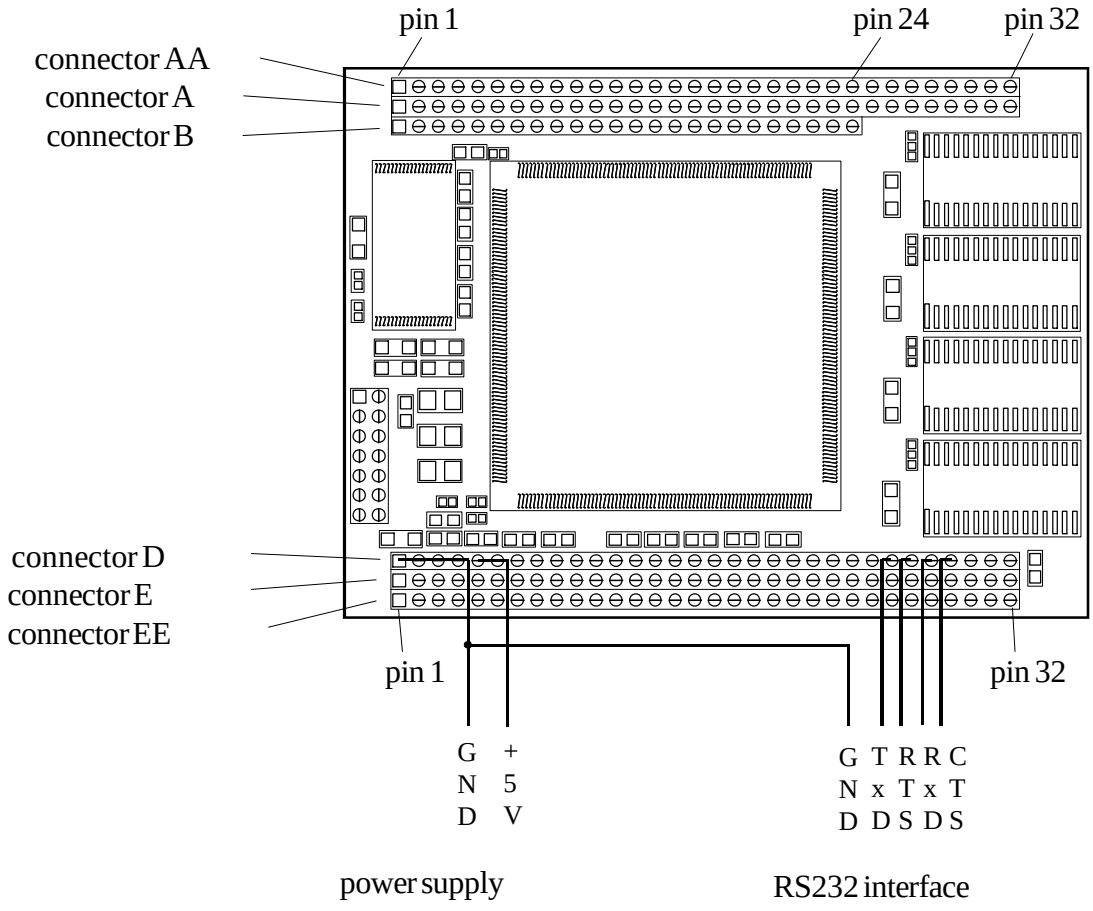
The C44CPU board is a high-performance embedded system from the ORSYS micro-line® xxCPU product family of modern Digital Signal Processor (DSP) boards. The C44CPU operates with a Texas Instruments 32-bit floating-point TMS320C44 signal processor. The TMS320C44 signal processor provides an extraordinary powerful Arithmetic Logic Unit (ALU) which performs additions, multiplications, divisions and root functions with hardware support in just one clock cycle. The TMS320C44 processor's multiplier operates with an accuracy of 40 bits (floating-point) or 2 x 32 bits with a 64-bit result (integer). The ALU accuracy is 40 bits (floating-point) or 32 bits (integer). The CPU core furthermore has a 32-bit barrel shifter and two independent address calculation units in order to execute parallel commands by several operands.
The local and global address width is 2 x 24 bits and enables a maximum memory size of 2 x 16M words. The available processor speeds are 40, 50, 60 and 80 MHz.
Additionally to the TMS320C44 processor's internal 2K-word RAM, there are two external static 0-wait state RAM banks with optionally 2 x 32K words (256 kbytes) or 2 x 128K words (1 Mbyte) as program and data memory available. The RAM banks can be buffered via the internal 128-words deep program cache memory of the TMS320C44 processor. The size of the flash EPROM boot memory is optionally either 128 kbytes or 512 kbytes.
Operations with ORSYS micro-line® systems are virtually problem-free. ORSYS processor boards are pin- and software compatible and price- and performance categorized . They are available with an extensive system software and universal peripheral components. ORSYS offers a powerful application end product which leads to a short development time, low development costs and a minimum development risk.

In order to operate the C44CPU board, developers don't need to have any knowledge about the processor memory map, the CPU mode or booting procedures . Developers always have the option to operate the processor in various modes or to use their own boot software. Basically, all necessary TMS320C44 signals are connected to the pins of the C44CPU board. Various solder bridges on the C44CPU board enable all processor modes.
This user's guide covers all C44CPU board functionalities. Details of the TMS320C44 signal processor can be found in the Texas Instruments TMS320C44 user's guide (with reference to the TMS320C4x user's guide).

1.2 Quick Start

Prior to operating, the following FILE software has to be copied to the development PC: DIR44.EXE, DIR44.SET, DEL44.EXE, DEL44.SET, REN44.EXE, REN44.SET, FORMAT44.EXE, FORMAT44.SET, CHKDSK44.EXE, CHKDSK44.SET, RUN44.EXE, RUN44.SET, FLOAD44.EXE, FLOAD44.SET, SLOAD44.EXE and SLOAD44.SET. The FILES can either be copied to a directory known to the system (e.g.: copy b:*.* c:\KNOWN_PATH) or a new directory can be established by the "md MICROLIN" (make directory) command. Now the FILES can be copied (cd MICROLIN, copy b:*.*). In order to make the program accessible from any directory, the command line PATH in the system FILE AUTOEXEC.BAT has to be extended by the new directory.

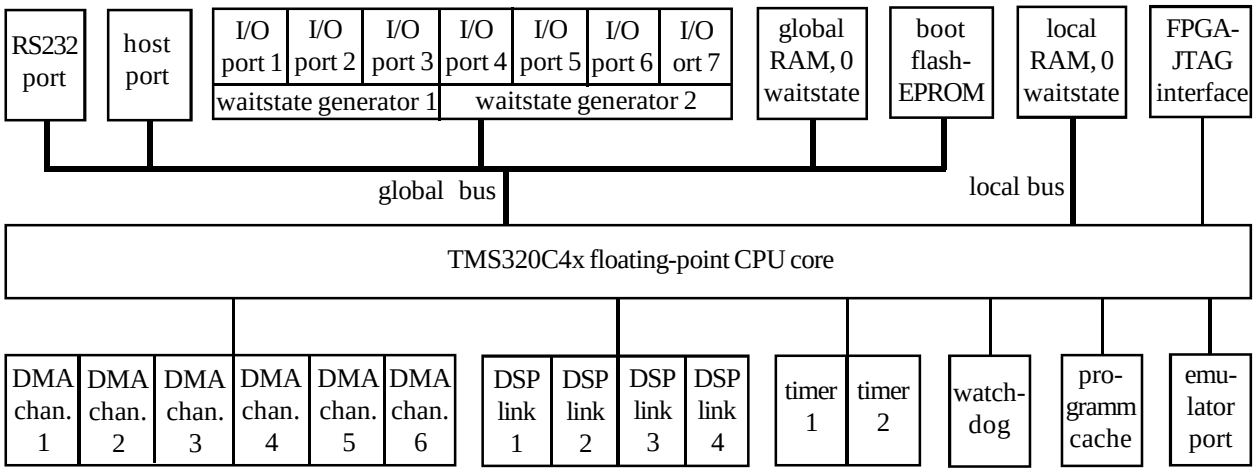
Prior to starting, the C44CPU board has to be supplied with +5V. In this case, the power supply has to be connected to the pins D1, D2, D3, D4 (ground) and D5, D6 (+5V). **Important:** The voltage supply must not exceed +5.5 V and **must not** be reversed, otherwise the C44CPU board could be permanently damaged.
The next step is to establish a RS232 connection between the development PC und the C44CPU board. The according pins on the C44CPU board are: D28 (RxD), D26 (TxD), D27 (RTS), D29 (CTS) and D1 (ground).
The pin-configuration on the 9-pole RS232 plug is: 2 (RxD), 3 (TxD), 7 (RTS), 8 (CTS) and 5 (ground). The RS232 cable between the C44CPU board and the PC has to be a null-modem cable (TxD (PC) -> RxD (C44CPU) and vica versa. The RTS and CTS lines have to be crossed respectively.



Now the C44CPU board can be connected to the power supply. The installed user program 'TOGGLE_LED' has to be booted automatically and the red and yellow LEDs have to toggle alternately. When executing the command 'DIRML', the development PC displays the C44CPU board directory which contains the 'TOGGLE_LED' user program. The command 'DIRML' can also choose the PC's requested COM port to be used. The syntax is 'DIRML' -Cx' (x = 1 or 2: used COM port).
If a XDS510 emulator or a compatible emulator is available for software development, there is no need for a RS232 connection to the development PC in order to start operating. In this case, the application software can be directly loaded from the emulator to the C44CPU board's RAM where it can be started (described in the emulator manual). In this case, the FILE software is not loaded to the C44CPU board. The RS232 interface is only required to activate the FILE software for residently storing the application program in the flash EPROM.

2. Hardware

2.1 C44CPU Block Diagram



2.2 Dual Bus Architecture

The used TMS320C44 processor provides two physically separated external buses (local bus and global bus). The program code fetch and data move can, for example, be executed externally by separate bus systems which leads to a significantly improved performance. Another possibility is to directly combine the global buses of several C44CPU boards to a shared memory in a multiprocessor configuration with up to eight boards. In this case, the global memory and the I/O space of each board are attached with a page on an increasing address space. Therefore, each processor has a direct access to the entire global RAM of all boards as well as to their I/O space. For implementing a shared memory system, it is necessary to have an external bus arbiter component in order to manage the hardware access rights.

2.3 RS232 Interface

The RS232 interface with its integrated line drivers is a communication interface between the development PC and the C44CPU board. The RS232 interface performs all downloading processes and FILE operations between the development PC and the C44CPU board. The RS232 interface can additionally be used as a universal interface for various applications. The SCC2691 device and the line drivers enable maximum asynchronous transfer rates of up to 115200 baud. The SCC2691 component data sheets are listed in the appendix.
The interface consists of the signal ports TxD (transmit), RxD (receive), RTS (request to send) and CTS (clear to send).
If the RS232 interface is not used, the SCC2691component as well as the line drivers can be switched to powerdown mode via software in order to reduce the power consumption. In this case, the 3.68 MHz output clock (pin E30) is deactivated.

2.4 Parallel Host Port

The parallel host port enables either a direct connection of two or several C44CPU boards or of one or several C44CPU boards to any host processor. The host port establishes a fast parallel bus connection between the communication partners. The C44CPU board is connected as a bus participant to the host processor just like a normal peripheral device and can be accessed via various registers. The implemented bus width on the board is 9 bits and can be extended to 32 bits with only one external device (see appenix). Here, the following control signals are available: HOST_OUT_CLK, /HOST_OUT_OE, HOST_IN_CLK and /HOST_IN_OE . The host port data exchange can be performed in polling, interrupt or DMA mode. The following lines belong to the host-port signals: HD0...HD8 (data), HA0...HA1 (addresses), /HEN (host port enable = chip select), /HRD (read), /HWR (write) and /HINT (interrupt).
If the host port is not needed for a specific application, it can alternatively be configurated to nine digital outputs or to four digital inputs and five digital outputs by respective software initialization.

2.5 I/O (Input/Output) Port 1...7

The altogether seven I/O (input/output) ports enable the simultaneous and direct connection of up to seven different customary peripheral boards (e.g. parallel-port devices, serial-port devices, clock boards, AD converters, display boards, etc.) without any additional external components. Timing differences between the fast signal processor and the normally slower peripheral boards can be offset by the two integrated programmable wait state generators. Wait state generator 1 controls the bus-timing of the I/O ports 1 to 3 and wait state generator 2 controls the bus-timing of the I/O ports 4 to 7. The number of wait states can be programmed via the wait state control registers 1and 2 . After a reset, the default value is 7 wait states each.
The I/O ports consist of the signal lines D0...D31 (data), A0...A23 (addresses), /CS1.../CS7 (chip select), /RD (read), /WR_0 (write), R/W_0 (read/write), /STRB_0 (Strobe), /INT0-IIOF0.../INT3-IIOF3 (interrupt), /IACK (interrupt acknowledge), /RESETOUT (reset, active low) and RESETOUT (reset, active high).
If necessary, the /IACK output pin can be pulsed within the interrupt routine by the assembler command 'IACK'.
The signal pair /RD_0 and /WR_0 is an alternative to the signal pair R/W_0 und /STRB_0. Either signal pair can be used, depending on the manufacturer and the type of the peripheral boards. As a rule, INTEL compatible boards require signal pair /RD_0 und /WR_0 and MOTOROLA compatible boards require signal pair R/W_0 und /STRB_0.

2.6 DSP Links

The TMS320C44 processor provides altogether four 8-bit wide link ports. Each of the four ports can transfer one byte per H1-clock. For the 40 MHz processor, the result is a transfer rate of 20 Mbytes per second per link; for the 50MHz processor, the rate is 25 Mbytes per second per link; for the 60 MHz type, the rate is 30 Mbytes per second per link and for the 80 MHz type the rate is 40 Mbytes per second per link. Each link port consists of the signal lines CnD0 to CnD7 (data), /CREQn (token request), /CACKn (token request acknowledge), /CSTRBn (data strobe), /CRDYn (data ready) and CDIR (direction). For the signal configuration, please refer to the informations provided in the Texas Instruments TMS320C4x user's guide (chapt.8-1 to 8-32). For link lines over 20 cm, it is furthermore recommended to buffer the data- and control signals via a driver (e.g. 74HC245). The data direction is determined by the CDIR signal. The ground connections between the processor board and the driver have to be short and thick.

2.7 DMA Coprocessor

The TMS320C44 processor integrated DMA coprocessor with its six separate DMA channels enables data transfer rates of up to hundreds of Mbytes/s. The DMA coprocessor can perform memory to memory transfers; transfers from I/O device to memory and vica versa; transfers between the communication link ports and memory; and transfers of single values to a block of memory. Prior to operating the DMA coprocessor, please refer to the initialization information provided in the Texas Instruments TMS320C4x user's guide (chapt.9-1 to 9-44).

2.8 Timer 0, Timer 1

The TMS320C44 processor has two programmable timers which can universally be used to generate application-specific clocks and system times. Besides the generation of periodical interrupts, the two signal lines TCLK0 and TCLK1 can deliver the output signal of the respective timer. The two signal lines TCLK0 and TCLK1 can furthermore be used as timer clock inputs to count external events.
For detailed information, please refer to the Texas Instruments TMS320C4x user's guide (chapter 9-45 to 9-53).

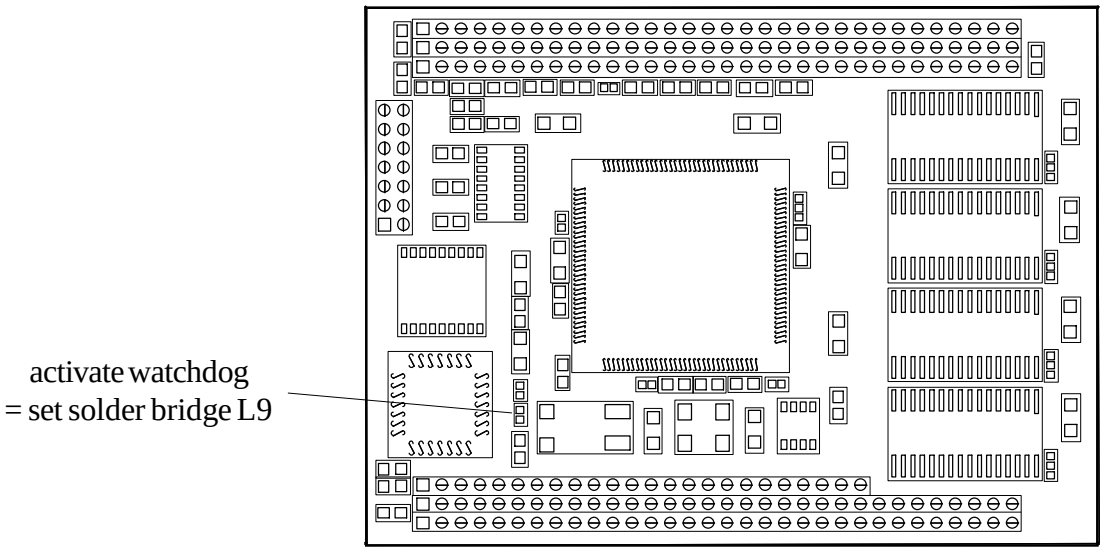
2.9 Auxiliary Timer

The SCC2691 peripheral device has an additional timer with a trigger function for periodical system interrupts. The SCC2691 is also used as serial interface . The FILE handling of the external development PC via the SCC2691 is not impaired by the timer function and does not have to be considered when the timer is activated. The SCC2691 data sheets are listed in the appendix.

2.10 Reset Generator, Watchdog

The C44CPU board provides a reset generator which generates a defined reset pulse during power ON, during a manual reset (e.g. with a /RESETIN-pin switch), during a power supply drop below 4.65V or in case of a watchdog event. The generated reset pulse has a duration of at least 140 ms and activates the /RESETOUT and RESETOUT lines during the 140 ms period. The watchdog is activated by solder bridge L9 . If the watchdog is not required, solder bridge L9 remains open *(default state = watchdog not active)*. The maximum watchdog retrigger interval is 1.6 seconds. A system reset pulse is generated after every exceeded retrigger interval. The watchdog is retriggered by a read- or write access to the SCC2691 device on the following addresses:

0x8022C000...0x8022C007 (global memory page 0) = *default stateafter delivery*
0x8026C000...0x8026C007 (global memory page 1)
0x802AC000...0x802AC007 (global memory page 2)
0x802EC000...0x802EC007 (global memory page 3)
0x8032C000...0x8032C007 (global memory page 4)
0x8036C000...0x8036C007 (global memory page 5)
0x803AC000...0x803AC007 (global memory page 6)
0x803EC000...0x803EC007 (global memory page 7)



2.11 Memory Map

2.11.1 RAM

The complete 32-bit wide organized RAM can be used for program- and data storing. This applies to the local- as well as to the global RAM. A large number of memory allocations can be selected due to the dual bus architecture on a single processor system program code and data areas can be splitted and freely devided by the local- and the global bus. It is often of advantage to exchange fast throughput data (e.g. during DMA operations) on a bus system, while on the second bus system the program code is simultanously operated without any speed losses. When no large data blocks are transfered within a single processor system, it is recommended to allocate the program code to the local RAM and data to the global RAM in order to achieve the maximum speed.

Due to speed reasons, only the generally used global variables should be allocated to the global bus for shared memory systems via the global RAM. All other variables shoul be allocated to the local bus together with the program code.
The allocation of the program code and data to the local- or the global RAM is exclusively performed by allocating the program code and data to the respective address space. Address space 0x00000000 to 0x7FFFFFFF addresses the local RAM and address space 0x80000000 to 0xFFFFFFFF the global RAM (and I/O).

The C44CPU board is available in two RAM versions:

0 wait state RAM:

1.) 2 x 32K words = 64K words (256 kbytes)
2.) 2 x 128K words = 256K words (1Mbyte)

Besides the two external RAM banks**,** the TMS320C44 processor has two additional internal RAM blocks with an altogether 2K-word (8 kbyte) deep memory.

2.11.2 Flash EPROM

The flash EPROM is the system's boot memory. It contains all user programs when the processor is in bootloader mode. The flash EPROM should **not** be directly read or written from the user program, it is directly handled by the boot program or the FILE system software. The C44CPU board provides an integrated protection mechanism to ensure the data security of the flash EPROM and to avoid an accidental deletion of the user programs. All programs necessary for booting, download operations and FILE handling are residently stored in the flash EPROM. The stored programs cannot be deleted.

The C44CPU board supports two flash EPROM versions:

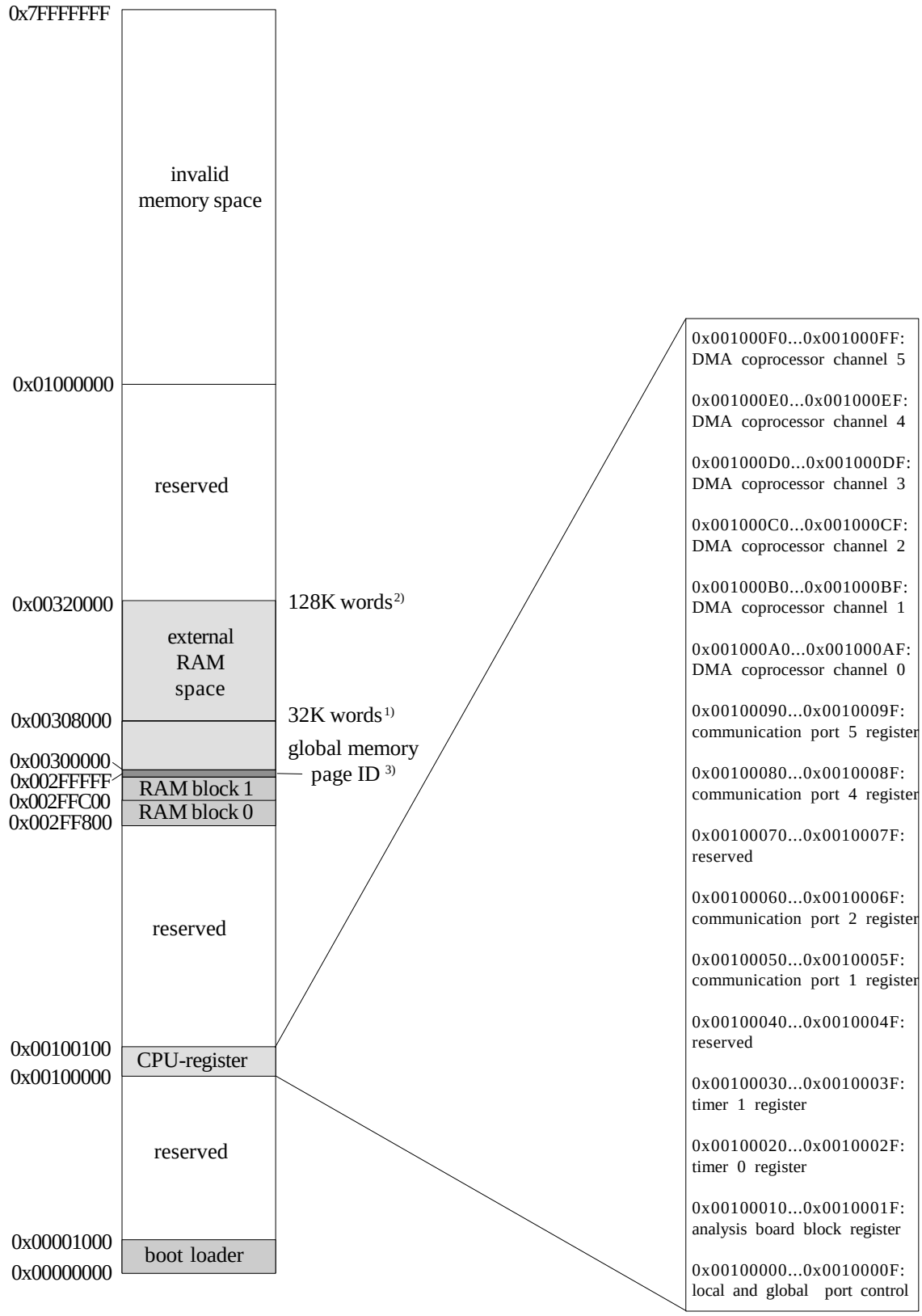
1.) 128 kbytes
2.) 512 kbytes

2.11.3 Program Cache

The TMS320C44 processor has an integrated 128-word program cache memory to buffer instructions which were read from the external RAM. When using the cache memory, the processor speed improves and the processor achieves optimum results for its internal parallel resources . The TMS320C44 cache memory is divided into four 32-word segments which are separately checked for any chache misses. This means that after a failed cache access, the maximum reconstruction of the cache contents is only one quarter of the cache while the other program words (three quarters) remain unchanged in the cache memory.

In order to activate the cache memory, bit 11 CE (Cache Enable) of the TMS320C44 processor status register has to be set.

2.12 C44CPU Memory Model Local Bus



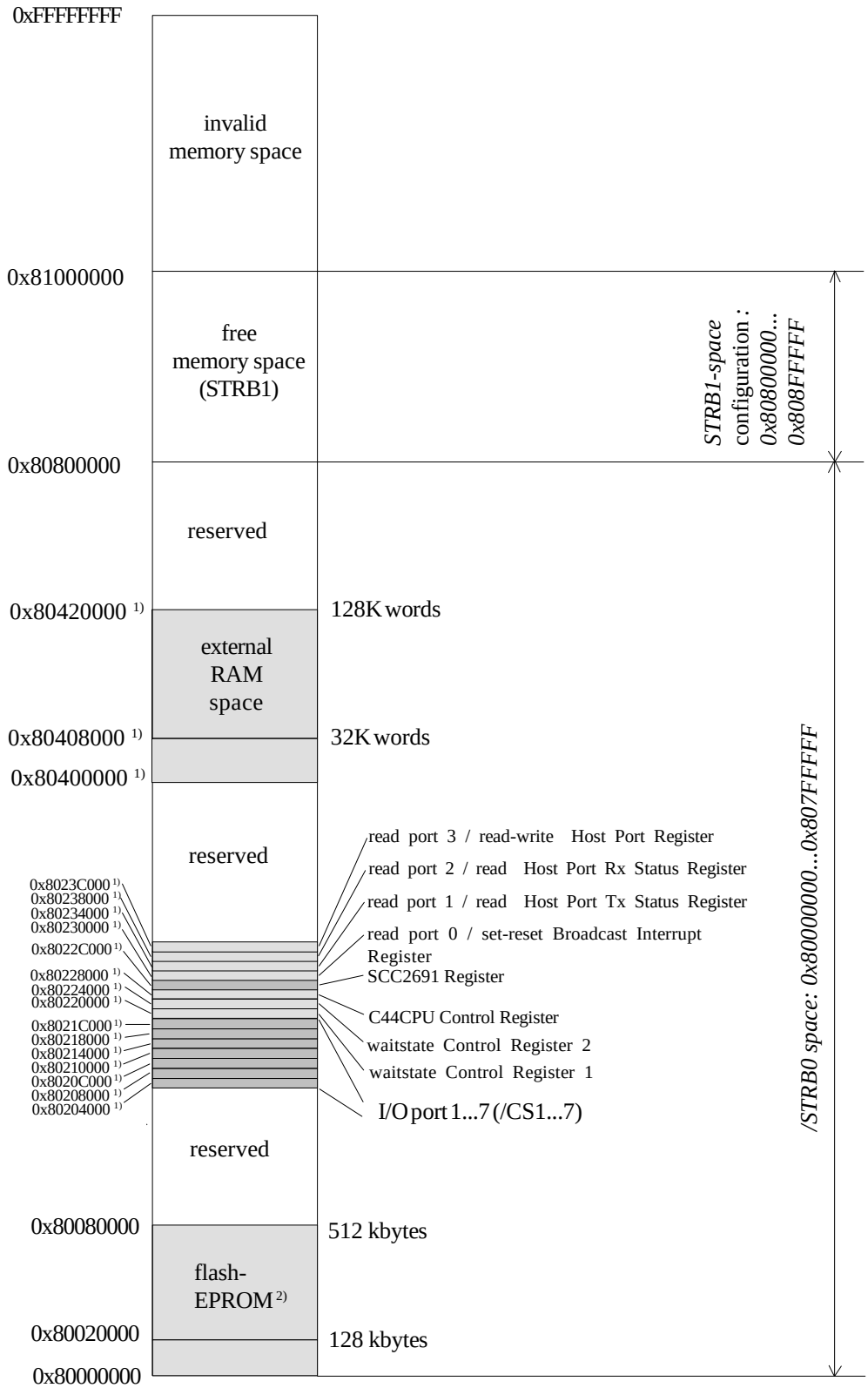
The local memory space is not affected by the global memory page configuration

1) = 0x00307E00...0x00307FFF is reserved on the 2 x 32K-word RAM equipment

2) = 0x0031FE00...0x0031FFFF is reserved on the 2 x 128K- word RAM equipment

3) = for global memory page recognition (0...7) reserved for software requests (entered by the boot system)

2.13 C44CPU Memory Model Global Bus



1) = addresses are only valid for global memory page = 0 *(= default state after delivery)*

2) = the access to the flash EPROM space by external busmasters is blocked

2.14 Global Memory Page 0...7, Shared Memory

The C44CPU board has an integrated memory-page mechanism which enables that up to eight boards can directly be coupled with each other via the global bus in order to implement a shared memory multiprocessor architecture. A separate address space within the entire shared memory space is assigned to each C44CPU board when an increasing 'global memory page' from 0 to 7 is determined. Physically, the memory is located on the processor boards (global RAM). Logically, the memory is increasing in linear and can be addressed equally by each processor board. The entire shared memory increases if more processor boards are connected.
Additionally to the shared memory function, this bus coupling provides that the entire external I/O space (/CS0...7, SCC2691, host port, etc.) of each processor board can be addressed equally by any other processor board.
Furthermore, additional external shared memory components can be coupled in order to meet application-specific requirements.
Via the global bus, each processor can trigger an interrupt signal or set a polling bit to any other processor as handshake between the processors.

The C44CPU board's data - and address buses are directly connected with each other in order to implement this multiprocessor architecture. The control lines /DE, /AE, /LOCK, STAT0...3, R/W, /STRB, /RDY, PAGE and /CE can each be connected with a suitable, external bus arbiter unit. ORSYS provides a respective bus-arbiter unit as FPGA solution.

2.14.1 RAM Addresses: global memory pages 0...7

global RAM (32K word RAM equipment)

0x80400000...0x80407FFF (global memory page 0)
0x80408000...0x8040FFFF (global memory page 1)
0x80410000...0x80417FFF (global memory page 2)
0x80418000...0x8041FFFF (global memory page 3)
0x80420000...0x80427FFF (global memory page 4)
0x80428000...0x8042FFFF (global memory page 5)
0x80430000...0x80437FFF (global memory page 6)
0x80438000...0x8043FFFF (global memory page 7)

global RAM (128K word RAM equipment)

0x80400000...0x8041FFFF (global memory page 0)
0x80420000...0x8043FFFF (global memory page 1)
0x80440000...0x8045FFFF (global memory page 2)
0x80460000...0x8047FFFF (global memory page 3)
0x80480000...0x8049FFFF (global memory page 4)
0x804A0000...0x804BFFFF (global memory page 5)
0x804C0000...0x804DFFFF (global memory page 6)
0x804E0000...0x804FFFFF (global memory page 7)

default state = global memory page = 0

2.14.2 I/O Port Addresses: global memory pages 0...7

I/O Port 1 (/CS1)

0x80204000...0x80207FFF	(global memory page 0)
0x80244000...0x80247FFF	(global memory page 1)
0x80284000...0x80287FFF	(global memory page 2)
0x802C4000...0x802C7FFF	(global memory page 3)
0x80304000...0x80307FFF	(global memory page 4)
0x80344000...0x80347FFF	(global memory page 5)
0x80384000...0x80387FFF	(global memory page 6)
0x803C4000...0x803C7FFF	(global memory page 7)

I/O Port 2 (/CS2)

0x80208000...0x8020BFFF	(global memory page 0)
0x80248000...0x8024BFFF	(global memory page 1)
0x80288000...0x8028BFFF	(global memory page 2)
0x802C8000...0x802CBFFF	(global memory page 3)
0x80308000...0x8030BFFF	(global memory page 4)
0x80348000...0x8034BFFF	(global memory page 5)
0x80388000...0x8038BFFF	(global memory page 6)
0x803C8000...0x803CBFFF	(global memory page 7)

I/O Port 3 (/CS3)

0x8020C000...0x8020FFFF	(global memory page 0)
0x8024C000...0x8024FFFF	(global memory page 1)
0x8028C000...0x8028FFFF	(global memory page 2)
0x802CC000...0x802CFFFF	(global memory page 3)
0x8030C000...0x8030FFFF	(global memory page 4)
0x8034C000...0x8034FFFF	(global memory page 5)
0x8038C000...0x8038FFFF	(global memory page 6)
0x803CC000...0x803CFFFF	(global memory page 7)

I/O Port 4 (/CS4)

0x80210000...0x80213FFF	(global memory page 0)
0x80250000...0x80253FFF	(global memory page 1)
0x80290000...0x80293FFF	(global memory page 2)
0x802D0000...0x802D3FFF	(global memory page 3)
0x80310000...0x80313FFF	(global memory page 4)
0x80350000...0x80353FFF	(global memory page 5)
0x80390000...0x80393FFF	(global memory page 6)
0x803D0000...0x803D3FFF	(global memory page 7)

I/O Port 5 (/CS5)

0x80214000...0x80217FFF	(global memory page 0)
0x80254000...0x80257FFF	(global memory page 1)
0x80294000...0x80297FFF	(global memory page 2)
0x802D4000...0x802D7FFF	(global memory page 3)
0x80314000...0x80317FFF	(global memory page 4)
0x80354000...0x80357FFF	(global memory page 5)
0x80394000...0x80397FFF	(global memory page 6)
0x803D4000...0x803D7FFF	(global memory page 7)

I/O Port 6 (/CS6)

0x80218000...0x8021BFFF	(global memory page 0)
0x80258000...0x8025BFFF	(global memory page 1)
0x80298000...0x8029BFFF	(global memory page 2)
0x802D8000...0x802DBFFF	(global memory page 3)
0x80318000...0x8031BFFF	(global memory page 4)
0x80358000...0x8035BFFF	(global memory page 5)
0x80398000...0x8039BFFF	(global memory page 6)
0x803D8000...0x803DBFFF	(global memory page 7)

I/O Port 7 (/CS7)

0x8021C000...0x8021FFFF	(global memory page 0)
0x8025C000...0x8025FFFF	(global memory page 1)
0x8029C000...0x8029FFFF	(global memory page 2)
0x802DC000...0x802DFFFF	(global memory page 3)
0x8031C000...0x8031FFFF	(global memory page 4)
0x8035C000...0x8035FFFF	(global memory page 5)
0x8039C000...0x8039FFFF	(global memory page 6)
0x803DC000...0x803DFFFF	(global memory page 7)

default state = global memory page = 0

2.14.3 External Register Addresses: global memory pages 0...7

Wait State Control Register 1

0x80220000...0x80223FFF	(global memory page 0)
0x80260000...0x80263FFF	(global memory page 1)
0x802A0000...0x802A3FFF	(global memory page 2)
0x802E0000...0x802E3FFF	(global memory page 3)
0x80320000...0x80323FFF	(global memory page 4)
0x80360000...0x80363FFF	(global memory page 5)
0x803A0000...0x803A3FFF	(global memory page 6)
0x803E0000...0x803E3FFF	(global memory page 7)

Wait State Control Register 2

0x80224000...0x80227FFF	(global memory page 0)
0x80264000...0x80267FFF	(global memory page 1)
0x802A4000...0x802A7FFF	(global memory page 2)
0x802E4000...0x802E7FFF	(global memory page 3)
0x80324000...0x80327FFF	(global memory page 4)
0x80364000...0x80367FFF	(global memory page 5)
0x803A4000...0x803A7FFF	(global memory page 6)
0x803E4000...0x803E7FFF	(global memory page 7)

C44CPU Control Register

0x80228000...0x8022BFFF	(global memory page 0)
0x80268000...0x8026BFFF	(global memory page 1)
0x802A8000...0x802ABFFF	(global memory page 2)
0x802E8000...0x802EBFFF	(global memory page 3)
0x80328000...0x8032BFFF	(global memory page 4)
0x80368000...0x8036BFFF	(global memory page 5)
0x803A8000...0x803ABFFF	(global memory page 6)
0x803E8000...0x803EBFFF	(global memory page 7)

SCC2691 Register

0x8022C000...0x8022FFFF	(global memory page 0)
0x8026C000...0x8026FFFF	(global memory page 1)
0x802AC000...0x802AFFFF	(global memory page 2)
0x802EC000...0x802EFFFF	(global memory page 3)
0x8032C000...0x8032FFFF	(global memory page 4)
0x8036C000...0x8036FFFF	(global memory page 5)
0x803AC000...0x803AFFFF	(global memory page 6)
0x803EC000...0x803EFFFF	(global memory page 7)

Read Port 0 / Set-Reset Broadcast Interr. Reg.

0x80230000...0x80233FFF	(global memory page 0)
0x80270000...0x80273FFF	(global Memory Pa/ge 1)
0x802B0000...0x802B3FFF	(global memory page 2)
0x802F0000...0x802F3FFF	(global memory page 3)
0x80330000...0x80333FFF	(global memory page 4)
0x80370000...0x80373FFF	(global memory page 5)
0x803B0000...0x803B3FFF	(global memory page 6)
0x803F0000...0x803F3FFF	(global memory page 7)

Read Port 1 / Read Host Port Tx Status Reg.

0x80234000...0x80237FFF	(global memory page 0)
0x80274000...0x80277FFF	(global memory page 1)
0x802B4000...0x802B7FFF	(global memory page 2)
0x802F4000...0x802F7FFF	(global memory page 3)
0x80334000...0x80337FFF	(global memory page 4)
0x80374000...0x80377FFF	(global memory page 5)
0x803B4000...0x803B7FFF	(global memory page 6)
0x803F4000...0x803F7FFF	(global memory page 7)

Read Port 2 / Read Host Port Rx Status Reg.

0x80238000...0x8023BFFF	(global memory page 0)
0x80278000...0x8027BFFF	(global memory page 1)
0x802B8000...0x802BBFFF	(global memory page 2)
0x802F8000...0x802FBFFF	(global memory page 3)
0x80338000...0x8033BFFF	(global memory page 4)
0x80378000...0x8037BFFF	(global memory page 5)
0x803B8000...0x803BBFFF	(global memory page 6)
0x803F8000...0x803FBFFF	(global memory page 7)

Read Port 3 / Read-Write Host Port Register

0x8023C000...0x8023FFFF	(global memory page 0)
0x8027C000...0x8027FFFF	(global memory page 1)
0x802BC000...0x802BFFFF	(global memory page 2)
0x802FC000...0x802FFFFF	(global memory page 3)
0x8033C000...0x8033FFFF	(global memory page 4)
0x8037C000...0x8037FFFF	(global memory page 5)
0x803BC000...0x803BFFFF	(global memory page 6)
0x803FC000...0x803FFFFF	(global memory page 7)

default state = global memory page = 0

2.15 I/O Register

The I/O space partly operates with 7 firmly adjusted wait states. This concerns the following registers:
- wait state control register 1
- wait state control register 2
- C44CPU control register
- SCC2691 register

The following host-port registers are firmly adjusted to 0 wait states:
- read port0 / set-reset broadcast interrupt register
- read port1 / read host port Tx status register
- read port2 / read host port Rx status register
- read port3 / read-write host port register

The wait states of the following I/O channels can be adjusted with the help of wait state control register 1:
- I/O port 1 (/CS1)
- I/O port 2 (/CS2)
- I/O port 3 (/CS3)

The wait states of following I/O channels can be adjusted with the help of wait state control register 2:
- I/O port 4 (/CS4)
- I/O port 5 (/CS5)
- I/O port 6 (/CS6)
- I/O port 7 (/CS7)

The three STRB0 WTCNT bits (waitcount) in the global memory interface control register of the TMS320C44 processor must not be programmed to a larger number of wait states as there are in the wait state control registers 1 and 2.
The two STRB0 SWW bits (software wait mode) of the global memory interface control register should be left unchanged to binary ´1 1´.

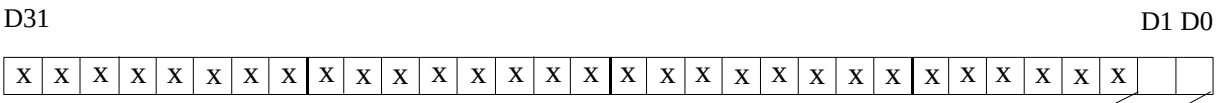
For global RAM shared memory systems, the busmaster processor board produces the necessary wait states even if it accesses the I/O space of another processor board. The number of inserted wait states in the I/O port space 1 to 7 (/CS1 to /CS7) depends on the adjusted wait states of the busmaster processor board and not on the adjusted wait states of the accessed processor board.

I/O Port 1 to I/O Port 7:

- address: 0x80204000...0x80207FFF [1)] (/CS1), I/O port 1: freely usable
- address: 0x80208000...0x8020BFFF [1)] (/CS2), I/O port 2: freely usable
- address: 0x8020C000...0x8020FFFF [1)] (/CS3), I/O port 3: freely usable
- address: 0x80210000...0x80213FFF [1)] (/CS4), I/O port 4: freely usable
- address: 0x80214000...0x80217FFF [1)] (/CS5), I/O port 5: freely usable
- address: 0x80218000...0x8021BFFF [1)] (/CS6), I/O port 6: freely usable
- address: 0x8021C000...0x8021FFFF [1)] (/CS7), I/O port 7: freely usable

[1)] = addresses are only valid for global memory page = 0 *(= default state after delivery)*

Wait State Control Register 1:

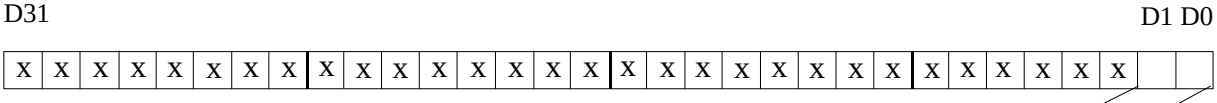


x = not used

D1	D0	I/O port 1,2,3
0	0	0 wait states
0	1	1 wait state
1	0	4 wait states
1	1	7 wait states

- address: 0x80220000 [1)]
- only writable, not readable
- 7 wait states after reset
- both STRB0 SWW bits (software wait mode) of the TMS320C44 global memory interface control register should be set

Wait-State Control Register 2:



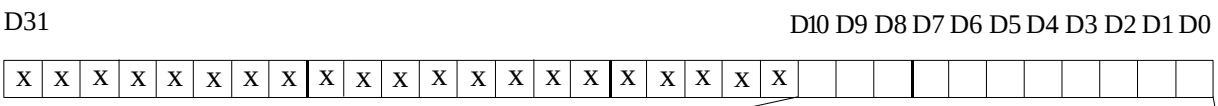
x = not used

D1	D0	I/O port 4,5,6,7
0	0	0 wait states
0	1	1 wait state
1	0	4 wait states
1	1	7 wait states

- address: 0x80224000 [1)]
- only writable, not readable
- 7 wait states after reset
- both STRB0 SWW bits (software wait mode) of the TMS320C44 global memory interface control register should be set

[1)] = addresses are only valid for global memory page = 0 *(= default state after delivery)*

C44CPU Control Register:



x =not used

Bit	0	1
D0	*HD0...HD8 = host port*	HD0...HD8 = port pin
D1	*port pins HD0...HD3 are inputs*	port-pins HD0...HD3 are outputs
D2	*host-port transmit interrupt disabled*	host-port transmit interrupt enabled
D3	*host-port receive interrupt disabled*	host-port receive interrupt enabled
D4	*INT1...3-IIOF1...3 pins = inputs* [1)]	INT1...3-IIOF1...3 pins = outputs
D5	*PC-FILE operations disabled*[2)]	PC-FILE operations possible
D6	*red LED OFF*	red LED ON
D7	*board operation*	hardware reset
D8	*RS232 driver active*	RS232 driver shutdown
D9	*disable broadcast interrupt*	enable broadcast interrupt
D10	*yellow LED OFF*	yellow LED ON

- address: 0x80228000 [1)]
- only writable, not readable
- *default state after reset*

[1)] = default state when using signals INT1-IIOF1, INT2-IIOF2 and INT3-IIOF3 as interrupt pins. The function of signal pins INT0-IIOF0 can only be initialized in the IIF (interrupt flag) register of the TMS320C44 processor (see TMS320C4x user´s guide, pages 3-12).

[2)] = when PC-FILE operation is disabled, all FILE commands, e.g. DIRML (after entering them on the development PC) can only be executed by a manually triggered reset signal on the C44CPU board.

[1)] = addresses are only valid for global memory page = 0 *(= default state after delivery)*

SCC2691Register (see data sheet SCC2691 in the appendix):

MR1 (Mode Register 1) and MR2 (Mode Register 2):
- address: 0x8022C000 [1)]
- both registers are writable and readable

SR (Status Register) and CSR (Clock Select Register):
- address: 0x8022C001 [1)]
- SR readable, CSR writable

CR (Command Register) and Test Register 1:
- address: 0x8022C002 [1)]
- test register 1 readable, CR writable

RHR (Receive Holding Register) and THR (Transmit Holding Register):
- address: 0x8022C003 [1)]
- RHR readable, THR writable

ACR (Auxiliary Control Register) and Test Register 2:
- address: 0x8022C004 [1)]
- test register 2 readable, ACR writable

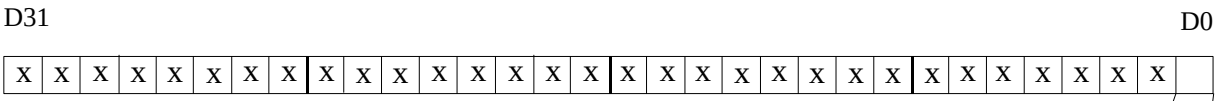
ISR (Interrupt Status Register) and IMR (Interrupt Mask Register):
- address: 0x8022C005 [1)]
- ISR readable, IMR writable

CTU (Counter / Timer Upper) and CTUR (Counter / Timer Upper Register):
- address: 0x8022C006 [1)]
- CTU readable, CTUR writable

CTL (Counter / Timer Lower) and CTLR (Counter / Timer Lower Register):
- address: 0x8022C007 [1)]
- CTL readable, CTLR writable

[1)] = addresses are only valid for global memory page = 0 *(= default state after delivery)*

Read Port 0 / Set-Reset Broadcast Interrupt Register



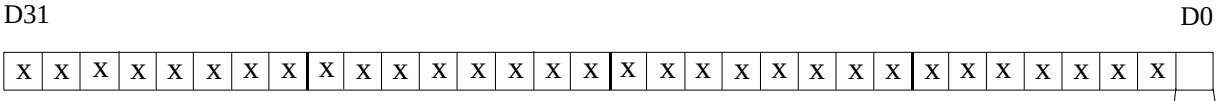
x = not used

Port Pin Function:	
HD0 (input)	D0
0	0
1	1

Host-Port Function:	
broadcast interrupt:	D0
force broadcast interrupt	1
release broadcast Interrupt	0

- address: 0x80230000[1)]
- only readable if the host port is switched to port-pin function (C44CPU control register bit D0 = 1) and if the host-port pins HD0...HD3 are switched to inputs (C44CPU control register bit D1 = 0)
- HD4...HD8 are always outputs if configured to port-pin function
- only writable (broadcast interrupt) if the host port is activated (C44CPU control register bit D0 = 1) A broadcast interrupt can be triggered via software, e. g. via the global bus of an external busmaster which affects the processor interrupt IIOF1. The broadcast interrupt bit **has** to be reset in the interrupt program.

Read Port 1 / Read Host Port Tx Status Register



x = not used

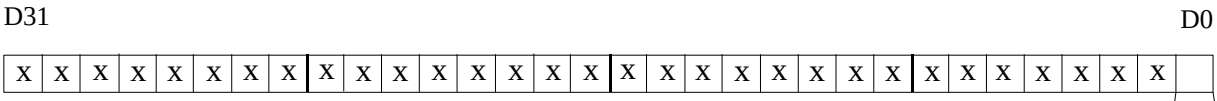
Port-Pin Function:	
HD1 (input)	D0
0	0
1	1

Host-Port Function:	
read host port Tx status	D0
Tx buffer empty	1
Tx buffer full	0

- address: 0x80234000 [1)]
- only readable, not writable
- HD4...HD8 are always outputs if configured to port-pin function
- port-pin function (input), if C44CPU control register bits D0 = 1 and D1 = 0; host port function if C44CPU control register bit D0 = 0

[1)] = addresses are only valid for global memory page = 0 *(= default state after delivery)*

Read Port 2 / Read Host Port Rx Status Register



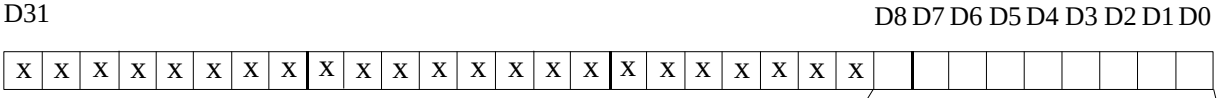
x = not used

Port-Pin Function:	
HD2 (input)	D0
0	0
1	1

Host-Port Function:	
read host port Rx status	D0
Rx buffer full	1
Rx buffer empty	0

- address: 0x80238000 [1)]
- only readable, not writable
- HD4...HD8 are always outputs if configured to port-pin function
- port-pin function (input) if C44CPU control register bits D0 = 1 and D1 = 0
- host-port function if C44CPU control register bit D0 = 0

Read Port 3 / Read-Write Host-Port Register



x = not used

Port-Pin Function (input):	
HD3 (input)	D0
0	0
1	1

Host-Port Function:
host-port data register
write data to HD0...HD8
read data from HD0...HD8

Port-Pin Function (output):
D0...D8 -> port pin HD0...HD8

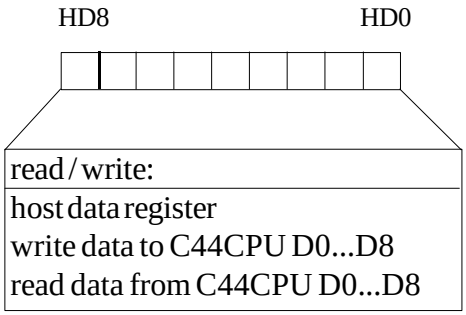
- address: 0x8023C000 [1)]
- if port-pin function and output, D0...D8 are only writable, not readable
- HD4...HD8 are always outputs if port-pin function and only writable
- port-pin function (HD3 = input) if C44CPU control register bits D0 = 1 and D1 = 0
- port-pin function (HD0...HD8 = output) if C44CPU control register bits D0 = 1 and D1 = 1
- with the reset signal, all port-pin outputs are internally set to ´1´
- host-port function, if C44CPU control register bit D0 = 0

[1)] = addresses are only valid for global memory page = 0 *(= default state after delivery)*

2.16 Host-Port Register (Host Side)

The host-port registers are the four C44CPU registers which can be addressed by the connected host processor. They are decoded by the respective selection of the C44CPU host processor address ports HA0 and HA1. The host address 0x01 is reserved and should not be addressed.

Host Data Register

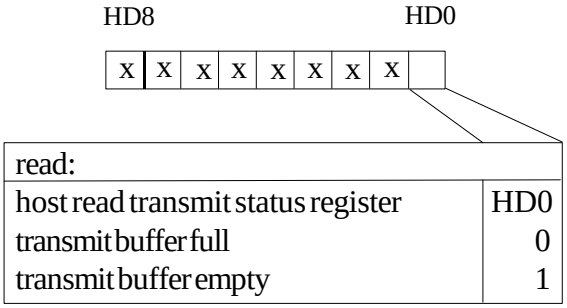


read / write:
host data register
write data to C44CPU D0...D8
read data from C44CPU D0...D8

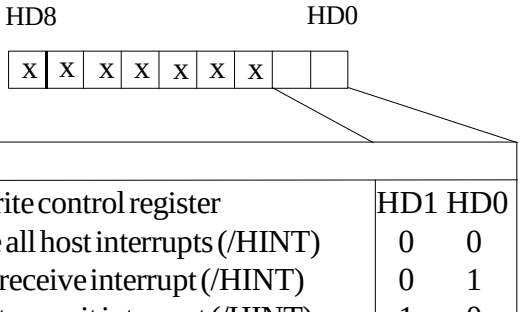
- host address: 0x00
- readable (read data from C44CPU) and writable (transmit data to C44CPU)
- only usable if C44CPU control register bit D0 = 0

Host Read Transmit Status Register / Host Write Control Register

x = not used



read:	
host read transmit status register	HD0
transmit buffer full	0
transmit buffer empty	1

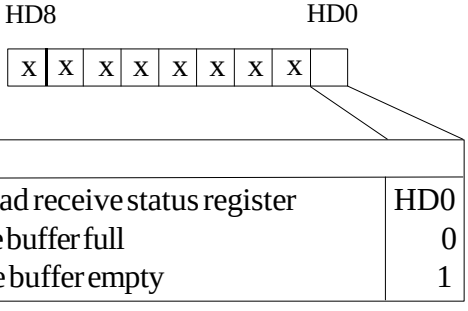


write:		
host write control register	HD1	HD0
disable all host interrupts (/HINT)	0	0
enable receive interrupt (/HINT)	0	1
enable transmit interrupt (/HINT)	1	0
enable both interrupts (/HINT)	1	1

- host address: 0x02
- all interrupts are disabled after reset
- only usable if C44CPU control register bit D0 = 0

Host Read Receive Status Register

x = not used



read:	
host read receive status register	HD0
receive buffer full	0
receive buffer empty	1

- host address: 0x03
- only usable if C44CPU control register bit D0 = 0

2.17 Interrupts

Additionally to the processor´s internal interrupt sources, the C44CPU board provides four external interrupt lines (/INT0-IIOF0 to /INT3-IIOF3) on the micro-line® bus as well as interupt triggering for the broadcast interrupt, the host-port interrupt and the RS232 interface. After asserting the low signal, the external interrupt lines trigger a respective interrupt on the processor . The signals can either be acitvated or disabled in the processor's IF (Interrupt Flag) register and can optionally be programmed as edge- and state triggered inputs.
The CPU interrupt signals IIOF1, IIOF2 and IIOF3 have a double function on the C44CPU board: 1) they are located on the pin for the external hardware interrupt and 2) additional board-internal interrupt sources are eventually also switched to the interrupt lines (see the following table).

CPU interrupt	interrupt source 1	interrupt source 2
IIOF0	/INT0-IIOF0 pin	-
IIOF1	/INT1-IIOF1 pin	broadcast interrupt
IIOF2	/INT2-IIOF2 pin	host-port interrupt
IIOF3	/INT3-IIOF3 pin	RS232 interrupt

If necessary, the double-occupied interrupt sources can be determined by software via respective polling within the interrupt program.
For the host port, this is possible by querying the register 'read port 1 /read host port Tx status register' (transmit status) or 'read port 2 / read host port Rx status register' (receive status).
For the RS232 interface, the status register SR of the SCC2691 device can be queried.
For the broadcast interrupt, polling can only be performed via the additional external interrupt souce.

2.18 Port-Pins

Some pins of unused interfaces can freely be used as programmable digital input/output ports.

Timer 0 and Timer 1Lines

The lines TCLK0 and TCLK1 of the TMS320C44 processor can be used as digital input/output ports if the external timer function is not used.

Parallel Host Port

The lines HD0 HD8 can be used as a digital output port by respective initialization of the C44CPU control register if the host port is not used. The lines HD0 to HD4 can alternatively be switched to digital input/ output ports by software.

Lines /INT0-IIOF0, /INT1-IIOF1, /INT2-IIOF2 and /INT3-IIOF3

The lines /INT0-IIOF0, /INT1-IIOF1, /INT2-IIOF2 and /INT3-IIOF3 can be used as digital input ports or as digital output ports. In the processor's IF (Interrupt Flag) register, the line /INT0-IIOF0 can be configured separately from port function (input or output) to interrupt function.
In the C44CPU control register, the lines /INT1-IIOF1, /INT2-IIOF2 and /INT3-IIOF3 can only be switched commonly to either inputs or outputs. A mixed function of these lines is only possible for interrupt inputs and port-pin inputs and not for outputs. When the lines /INT1-IIOF1, /INT2-IIOF2 and /INT3-IIOF3 of the C44CPU control register are switched to outputs , the signal /INT0-IIOF0 can only be used as interrupt input.

An initialized combination where the lines /INT1-IIOF1, /INT2-IIOF2 and /INT3-IIOF3 are switched to inputs in the C44CPU control register and to outputs in the processor's IF (Interrupt Flag) register should be avoided.

2.19 LEDs

The C44CPU processor board has one green, one red and one yellow LED. The green LED is the visual control light for flash-EPROM accesses. It operates similar to the LEDs on the hard disk and flashes with every flash memory access. The red LED can be controlled by software and be switched ON or OFF by setting or resetting the bit D6 of the C44CPU control register. The yellow LED can also be switched ON or OFF by bit D10 of the C44CPU control register.

2.20 Clock Frequency / Processor Performance

The C44CPU board 's available clock frequencies are 40, 50, 60 and 80 MHz. The resulting maximum processor performances are 40, 50, 60 and 80 MFLOPS (Million Floatingpoint Operations Per Second) or 20, 25, 30 and 40 MIPS (Million Instructions Per Second).

3. Software

3.1 Summary

The FILE system of the C44CPU board consists of the commands DIRML, DELML, RENML, FORMATML, CHKDSKML, RUNML, FLOAD44 and SLOAD44. All instructions are residently installed in the C44CPU board's flash EPROM and the corresponding commands are stored as .EXE and .SET FILES on the development PC. In order to execute a FILE command, the respective command, e. g. DIRML, has to be entered on the development PC under MS-DOS (3.3 or higher). The communication with the C44CPU board is carried out via the RS232 interface. After entering a command, the active user program on the C44CPU board is interrupted, the FILE system software is loaded, the command is executed and the active user program is restarted.
In order to select the requested COM interface of the development PC, the command can be entered with a parameter following, e. g. , DIRML -Cn (n = 1 or 2). The COM interface provided by the development PC will be stored and automatically used for all following commands. The commands DIRML-H or DIRML? start the help function. This applies to all FILE commands.

3.2 DIRML

The command DIRML lists the actual C44CPU board directory on the screen of the development PC including name, date, time and FILE size of the maximum 63 FILES. The autobooting user program and the remaining flash EPROM are additionally displayed.

3.3 DELML

The command (Delete) DELML <Name> deletes the entered FILE on the C44CPU board. The afterwards free memory space on the C44CPU board's flash EPROM becomes automatically available for other FILES.

3.4 RENML

The command (Rename) RENML <OldName NewName> replaces the name (OldName) of a FILE by a new name (NewName) on the C44CPU board. The maximum length of a FILE name is 15 characters.

3.5 FORMATML

The command FORMATML executes an unirrevocable formating of the flash EPROM on the C44CPU board. All user programs are deleted.

3.6 CHKDSKML

The command (Checkdisk) CHKDSKML executes a verification of every single FILE on the C44CPU board's flash EPROM . The result of the verification is the number of available FILES, as well as the complete memory and the still free flash EPROM displayed on the development PC screen.

3.7 RUNML

The command RUNML <Name> sets the status of the provided user program to autobooting and starts it on the C44CPU board. The program is automatically booted after every C44CPU board restart or reset.

3.8 FLOAD44

The command (Flash Load) FLOAD44 is a download program which loads a linker-produced application program to the C44CPU board after the conversion into the extended tektronix format (with the command C44CPU control register HEX30 <Name>) via the RS232 interface. The application program is residently stored on the C44CPU board as FILE including program name, date, time and program size. After the loading procedure, the program automatically has the status booting program and is started. The program is booted automatically after every C44CPU board restart or reset. The command FLOAD44 <Name> has to be entered on the development PC in order to perform the loading process.

3.9 SLOAD44

The command (Speed Load) SLOAD44 is a download program which temporary loads a linker-produced application program to the RAM of the C44CPU board after the conversion into the extended tektronix format (with the command HEX30 <Name>) via the RS232 interface. The command SLOAD44 <Name> has to be entered on the development PC in order to perform the loading process. The application program is first loaded and then started. The application program loaded by SLOAD44 is deleted if a C44CPU board restart or a reset occurs.

3.10 C-Compiler and Assembler

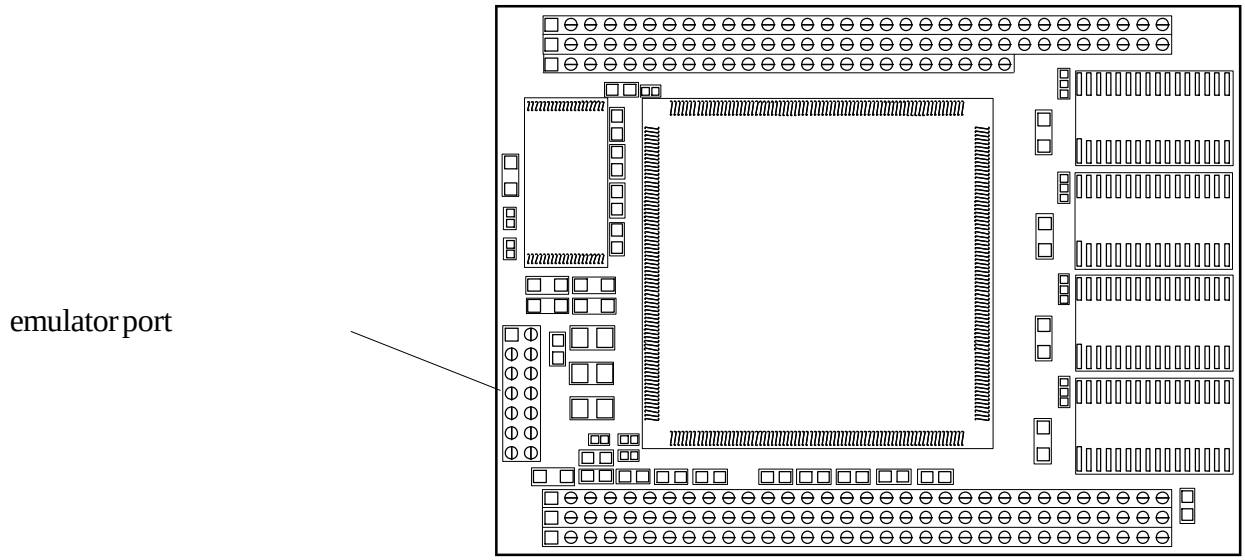
The standard software languages offered by Texas Instruments (TI) are available in two versions: The basic version consists of an assembler and a linker. The basic version is sufficient to implement C44CPU software projects in assembler programming language . The TI order number for the basic version is: TMDS3243850-02 (PC version).
The extended version consists of a ANSI C-compiler, assembler and linker. With the extended version, C44CPU software projects can be implemented in the C- and assembler programming languages. Single assembler lines can also be inlined into C-software projects or complete assembler algorithms can be integrated into C-software projects. The TI order number for the extended version is: TMDS3243855-02 (PC version). ORSYS provides both software packages.

3.11 C++ Compiler and ADA Compiler

Compilers for the program languages C++ and ADA are additionally available to the above listed software languages.

3.12 Emulator

TI as well as other providers offer several emulator systems for comfortable software debugging. Emulators usually consist of a PC-interface card which is connected to the C44CPU board emulator pin-connector by an emulator cabel to activate the C44CPU board's on-chip emulator. Emulators enable symbolic debugging with the follwing important debugging functions: breakpoints, single step, display of register contents as well as variable and memory contents, simultanous debugging of C- and assembler code, etc. A windows-oriented user interface facilitates the emulator handling . ORSYS provides the TI emulator package XDS510.



3.13 Simulator

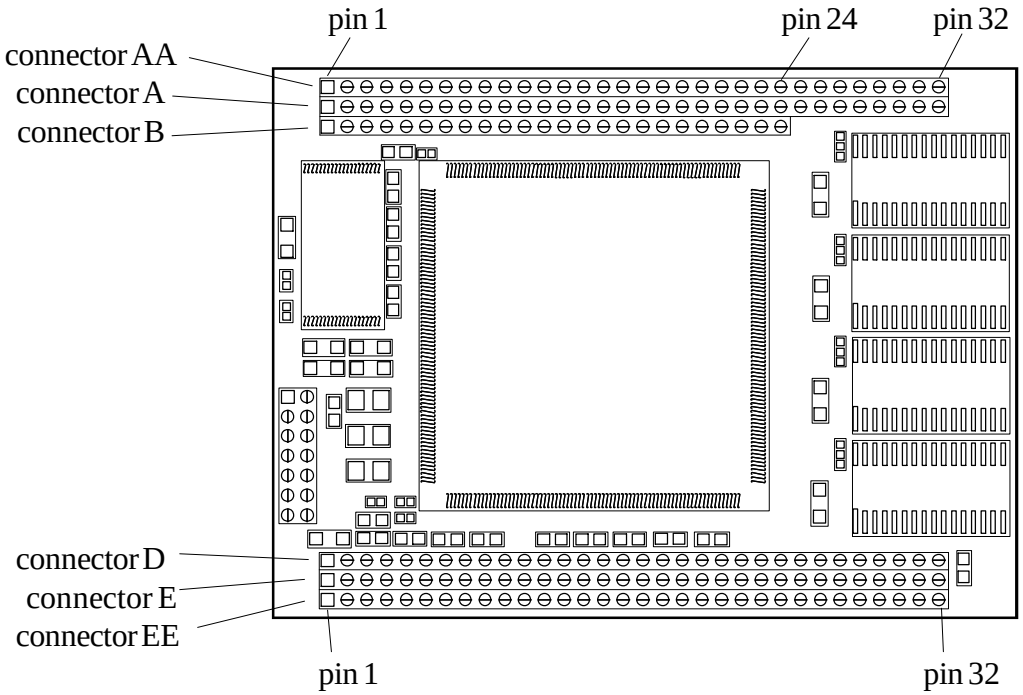
As an alternative to the emulator, the developed software can also be tested by a TI simulator. The simulator offers the same debugging techniques as the emulator and provides the same user interface. The difference in debugging between the emulator and the simulator is that the emulator actually performs the software on the C44CPU hardware and the simulator merely performs a target processor simultation on the PC. The TI order number for the simulator package is TMDS3245851-02 (PC version) and can be obtained from ORSYS.

3.14 Real-Time Operating Systems

For larger software projects, the real-time operation systems SPOX from SPECTRON and VIRTUOSO from EONIC SYSTEMS can be used for the C44CPU board. They are real-time multitasking operation systems with excellent results for Digital Signal Processors. Additionally to the operation system core, there are various libraries with mathematic functions or special DSP algorithms available which provide protocol communication with other host systems (e. g. MS-DOS, Windows, LynxOS, OS-9, SunOS and VxWorks).

4. Appendix

4.1 Pin-Configuration



pin	connector AA	conn.A	conn.B	conn.C	connector D	connector E	connector EE
1	/DE (I)	D00 (I/O/Z)	A00 (O/Z)	-	GND (I)	/HINT (O)	C2D0 (I/O)
2	/AE (I)	D01 (I/O/Z)	A01 (O/Z)	-	GND (I)	/HWR (I)	C2D1 (I/O)
3	/LOCK (0)	D02 (I/O/Z)	A02 (O/Z)	-	GND (I)	/HRD (I)	C2D2 (I/O)
4	STAT0 (0)	D03 (I/O/Z)	A03 (O/Z)	-	GND (I)	/HEN (I)	C2D3 (I/O)
5	STAT1 (0)	D04 (I/O/Z)	A04 (O/Z)	-	+5V (I)	HA1 (I)	C2D4 (I/O)
6	STAT2 (0)	D05 (I/O/Z)	A05 (O/Z)	-	+5V (I)	HA0 (I)	C2D5 (I/O)
7	STAT3 (0)	D06 (I/O/Z)	A06 (O/Z)	-	/RESETIN (I)	HD0 (I/O)	C2D6 (I/O)
8	R/W_1 (O/Z)	D07 (I/O/Z)	A07 (O/Z)	-	/RESETOUT (O)	HD1 (I/O)	C2D7 (I/O)
9	/STRB_1 (O/Z)	D08 (I/O/Z)	A08 (O/Z)	-	RESETOUT (O)	HD2 (I/O)	/CREQ2 (I/O)
10	/RDY_1 (I)	D09 (I/O/Z)	A09 (O/Z)	-	/CS1 (O)	HD3 (I/O)	/CACK2 (I/O)
11	PAGE_1 (O/Z)	D10 (I/O/Z)	A10 (O/Z)	-	/CS2 (O)	HD4 (I/O)	/CSTRB2 (I/O)
12	/CE_1 (I)	D11 (I/O/Z)	A11 (O/Z)	-	/CS3 (O)	HD5 (I/O)	/CRDY2 (I/O)
13	/CE_0 (I)	D12 (I/O/Z)	A12 (O/Z)	-	/CS4 (O)	HD6 (I/O)	CDIR2 (0)
14	/NMI (I)	D13 (I/O/Z)	A13 (O/Z)	-	/CS5 (O)	HD7 (I/O)	C4D0 (I/O)
15	C1D0 (I/O)	D14 (I/O/Z)	A14 (O/Z)	-	/CS6 (O)	HD8 (I/O)	C4D1 (I/O)
16	C1D1 (I/O)	D15 (I/O/Z)	A15 (O/Z)	-	/CS7 (O)	HOST_OUT_CLK (O)	C4D2 (I/O)
17	C1D2 (I/O)	D16 (I/O/Z)	A16 (O/Z)	-	/INT0-IIOF0 (I/O)	/HOST_OUT_OE (O)	C4D3 (I/O)
18	C1D3 (I/O)	D17 (I/O/Z)	A17 (O/Z)	-	/INT1-IIOF1 (I/O)	HOST_IN_CLK (O)	C4D4 (I/O)
19	C1D4 (I/O)	D18 (I/O/Z)	A18 (O/Z)	-	/INT2-IIOF2 (I/O)	/HOST_IN_OE (O)	C4D5 (I/O)
20	C1D5 (I/O)	D19 (I/O/Z)	A19 (O/Z)	-	/INT3-IIOF3 (I/O)	C5D0 (I/O)	C4D6 (I/O)
21	C1D6 (I/O)	D20 (I/O/Z)	A20 (O/Z)	-	/IACK (O/Z)	C5D1 (I/O)	C4D7 (I/O)
22	C1D7 (I/O)	D21 (I/O/Z)	A21 (O/Z)	-	/RD_0 (O)	C5D2 (I/O)	/CREQ4 (I/O)
23	/CREQ1 (I/O)	D22 (I/O/Z)	A22 (O/Z)	-	/WR_0 (O)	C5D3 (I/O)	/CACK4 (I/O)
24	/CACK1 (I/O)	D23 (I/O/Z)	A23 (O/Z)	-	R/W_0 (O/Z)	C5D4 (I/O)	/CSTRB4 (I/O)
25	/CSTRB1 (I/O)	D24 (I/O/Z)	-	-	/STRB_0 (O/Z)	C5D5 (I/O)	/CRDY4 (I/O)
26	/CRDY1 (I/O)	D25 (I/O/Z)	-	-	TXD (O)	C5D6 (I/O)	CDIR4 (0)
27	CDIR1 (0)	D26 (I/O/Z)	-	-	RTS (O)	C5D7 (I/O)	/CREQ5 (I/O)
28	TDO_FPGA (O)	D27 (I/O/Z)	-	-	RXD (I)	TCLK0 (I/O/Z)	/CACK5 (I/O)
29	TDI_FPGA (I)	D28 (I/O/Z)	-	-	CTS (I)	TCLK1 (I/O/Z)	/CSTRB5 (I/O)
30	TCK_FPGA (I)	D29 (I/O/Z)	-	-	/RDY_0 (I)	CLK_3,68MHZ (O)	/CRDY5 (I/O)
31	TMS_FPGA (I)	D30 (I/O/Z)	-	-	-	H1 (O)	CDIR5 (0)
32	VPP_FPGA (I)	D31 (I/O/Z)	-	-	-	-	/FLA_CS (I/O)

4.1.1 Pin-Description

Connector AA:

The connector AA is a specific C44CPU expansion connector which is not included in the micro-line® standard. This connector transmits only specific TMS320C44 signals to the outside. These signals are mostly global bus control- and C4x communication port signals.

/DE:
Global Data Bus Enable input (active low). The signal is low during normal C44CPU board operation. For multiprocessor systems with external busmaster, /DE has to be deactivated during external accesses in order to switch the data bus drivers into tristate. /DE is provided with a pulldown resistor on the C44CPU board. The pin remains open if there is a shared memory system with an uncoupled bus.

/AE:
Global Address Bus Enable input (active low). The signal is low during normal C44CPU board operation. For multiprocessor systems with external busmaster, /AE has to be deactivated during external accesses in order to switch the address bus drivers into tristate. /AE is provided with a pulldown resistor on the C44CPU board . The pin remains open if there is a shared memory system with an uncoupled bus.

/LOCK:
Global Bus Locking signal (output, active low). For multiprocessor systems, /LOCK can be activated during global memory accesses in order to stop the external bus arbiter from passing on the global bus. The pin remains open if there is no shared memory system on the global bus.

STAT0...STAT3:
These four output signals encode the momentary bus state of the TMC320C44 processor (see TMS320C4x user´s guide, pages 7-5). The pin remains open if there is no shared memory system on the global bus.

R/W_1:
Global bus memory interface 1 Read/Write output signal of the TMS320C44 processor. In high state, it signals an external read cycle and in the low state an external write cycle. The signal is only required if an external global bus memory expansion is implemented via memory interface 1. The pin remains open during normal operation. /R/W_1 is provided with a pullup resistor on the C44CPU board.

/STRB_1:
Global bus memory interface 1 Strobe output signal (active low) of the TMS320C31 processor. It signals a global bus read- or write access. The signal is only required if an external global bus memory expansion is implemented via memory interface 1. The pin remains open during normal operation. /STRB_1 is provided with a pullup resistor on the C44CPU board.

/RDY_1:
Global bus memory interface 1 Ready input signal (active low) of the TMS320C44 processor. For an additional memory interface 1 memory expansion, /RDY_1 can be used to insert additional wait states on external processor accesses by external hardware. /RDY_1 is provided with a pulldown resistor on the C44CPU board. The pin remains open during normal operation.

PAGE_1:
Global bus memory interface 1 page output signal (active high) of the TMS320C44 processor. For a memory interface 1 DRAM expansion, the signal can be used to transfer a new page address to the memory components by external hardware. /PAGE_1 is provided with a pulldown resistor on the C44CPU board. The pin remains open during normal operations.

/CE_1:
Global bus memory interface 1 Control Enable input (active low). The signal is low during normal C44CPU board operation. For multiprocessor systems with an external busmaster, /CE_1 has to be deactivated during external accesses. By deactivating /CE_1, the global bus control signals /STRB_1, PAGE_1 and R/W_1 are switched into tristate. /CE_1 is provided with a pulldown resistor on the C44CPU board . The pin remains open if there is no shared memory system on the global bus.

/CE_0:
Global bus memory interface 0 Control Enable input (active low). The signal is low during normal C44CPU board operation. For multiprocessor systems with an external busmaster, /CE_0 has to be deactivated during external accesses. By deactivating /CE_0, the global bus control signals /STRB_0, PAGE_0 and R/W_0 are switched into tristate. /CE_0 is provided with a pull-down resistor on the C44CPU board. The pin remains open if there is no shared memory system on the global bus.

/NMI:
Non-Maskable Interrupt input (negative edge triggered). The signal can be used to connect high-prioritised non-maskable interrupt signals to the TMS320C44 processor. /NMI is provided with a pullup resistor on the C44CPU board. The pin remains open during normal operations.

C1D0...C1D7:
Communication port 1 Data bus (bidirectional).

/CREQ1:
Communication port 1 Token Request (bidirectional).

/CACK1:
Communication port 1 Token Request Acknowledge (bidirectional).

/CSTRB1:
Communication port 1 Data Strobe (bidirectional).

/CRDY1:
Communication port 1 Data Ready (bidirectional).

CDIR1:
Communication port 1 Direction (output).

TDO_FPGA, TDI_FPGA, TCK_FPGA, TMS_FPGA, VPP_FPGA:
JTAG (IEEE 1149.1) interface to program the FPGA component.

Connector A:

D00...D31:
Bidirectional global bus data lines of the TMS320C44 processor.

Connector B:

A00...A23:
global bus address lines of the TMS320C44 processor.

Connector C:

Not provided on the C44CPU board.

Connector D:

GND:
Power supply: ground

+5V:
Power supply : +5V. The board asserts a reset signal for voltages below +4.65V. The valid maximum voltage is +5.5V.

/RESETIN:
Reset Input line (active low) for an external reset button. The signal does not have to be debounced. The required pullup resistor is integrated on the C44CPU board.

/RESETOUT:
Reset Output line (active low, no open collector) for external peripheral devices. The signal is activated with every C44CPU board reset.

RESETOUT:
Inverted /RESETOUT output signal (active high, no open collector).

/CS1:
Chip Select output (active low) of I/O port 1. /CS1 is activated during read- or write accesses to the I/O address space 0x80204000 [1)] to 0x80207FFF [1)]. The signal is decoded out of the global bus address and becomes valid after a FPGA delay to the address output.

/CS2:
Chip Select output (active low) of I/O port 2. /CS2 is activated during read- or write accesses to the I/O address space 0x80208000 [1)] to 0x8020BFFF [1)]. The signal is decoded out of the global bus address and becomes valid after a FPGA delay to the address output.

[1)] = addresses are only valid for global memory page = 0 *(= default state after delivery)*

/CS3:
Chip Select output (active low) of I/O port 3. /CS3 is activated during read- or write accesses to the I/O address space 0x8020C000 [1)] to 0x8020FFFF [1)]. The signal is decoded out of the global bus address and becomes valid after a FPGA delay to the address output.

/CS4:
Chip Select output (active low) of I/O port 4. /CS4 is activated during read- or write accesses to the I/O address space 0x80210000 [1)] to 0x80213FFF [1)]. The signal is decoded out of the global bus address and becomes valid after a FPGA delay to the address output.

/CS5:
Chip Select output (active low) of I/O port 5. /CS5 is activated during read- or write accesses to the I/O address space 0x80214000 [1)] to 0x80217FFF [1)]. The signal is decoded out of the global bus address and becomes valid after a FPGA delay to the address output.

/CS6:
Chip Select output (active low) of I/O port 6. /CS6 is activated during read- or write accesses to the I/O address space 0x80218000 [1)] to 0x8021BFFF [1)]. The signal is decoded out of the global bus address and becomes valid after a FPGA delay to the address output.

/CS7:
Chip Select output (active low) of I/O port 7. /CS7 is activated during read- or write accesses to the I/O address space 0x8021C000 [1)] to 0x8021FFFF [1)]. The signal is decoded out of the global bus address and becomes valid after a FPGA delay to the address output.

/INT0-IIOF0.../INT3-IIOF3:
Interrupt input lines (active low) of the TMS320C44 processor. All four interrupt inputs can optionally be either edge- or level triggered**.** An alternative to the interrupt function is to conifgurate the lines as universal input/output ports. The C44CPU board has one pullup resistor for each interrupt line. /INT0-IIOF0 must not be activated by an external device during a C44CPU board reset or while booting which means /INT0-IIOF0 must remain high.

/IACK:
Interrupt Acknowledge output signal (active low) of the TMS320C44 processor. The line can be pulsed within an interrupt routine by the software instruction IACK to acknowledge the interrupt at the requested system.

/RD_0:
Global bus memory interface 0 read signal (output , active low). The signal is always in low impedance state and cannot be switched into tristate. /RD _0 is in high state during internal read accesses of the TMS320C44 processor.

/WR_0:
Global bus memory interface 0 write signal (output, active low). The signal is always in low impedance state and cannot be switched into tristate. /WR_0 is in high state during internal write accesses of the TMS320C44 processor.

[1)] = addresses are only valid for global memory page = 0 *(= default state after delivery)*

R/W_0:
Global bus memory interface 0 Read/Write Output signal of the TMS320C44 processor. An external read cycle occurs if the signal is high and an external write cycle occurs if the signal is low.

/STRB_0:
Global bus memory interface 0 Strobe output signal (active low) of the TMS320C44 processor. It signals an external read- or write access.

TXD:
Transmit Data output of the RS232 interface. The required ± 10V line drivers are integrated on the C44CPU board.

RTS:
Request To Send output of the RS232 interface. The required ± 10V line drivers are integrated on the C44CPU board.

RXD:
Receive Data input of the RS232 interface. The required ± 10V line drivers are integrated on the C44CPU board.

CTS:
Clear To Send input of the RS232 interface. The required ± 10V line drivers are integrated on the C44CPU board.

/RDY_0:
Global bus memory interface 0 bus Ready input signal (active low). The signal can be used to insert additional I/O wait states on external accesses to the TMS320C44 processor. When activating the signal during an external memory access, all lines of the bus are statically stored until the /RDY_0 signal is inactive again. The pin remains open if the hardware does not produce any external wait states. The required pulldown resistor is integrated on the C44CPU board.

Connector E:

/HINT:
Host Port Interrupt output signal (active low). This signal can be used as interrupt input signal for a host processor.

/HWR:
Host Write input signal (active low). The signal can be connected with the /WR output signal of a host processor. The pin remains open if no host processor is connected.

/HRD:
Host Read input signal (active low). The signal can be connected with the /RD output signal of a host processor. The pin remains open if no host processor is connected.

/HEN:
Host Enable input signal (active low). The signal can be connected with the chip-select output signal (decoded address space) of a host processor. The C44CPU board has an integrated pullup resistor. The pin remains open if no host processor is connected.

HA0, HA1:
Host Address input signals. The signals can be connected with the address signals A0 and A1 of a host processor.

HD0...HD8:
Host Data input/output signals. In the host port mode, the signals can be connected with data ports D0...D8 of a host processor. In the port-pin mode, they are used as programmable, digital I/O (input/output) pins. After reset and configuring the port-pins to outputs, all signals are set to ´1´.

HOST_OUT_CLK:
Host Port Out clock signal (output, active low to high transition). This signal can be used to trigger an external latch device in transmit direction for expansions of the host-port interface.

/HOST_OUT_OE:
Host Port Out Output Enable signal (output, active low). This signal can be used to enable the output drivers of an external latch device in transmit direction for expansions of the host-port interface.

HOST_IN_CLK:
Host Port In Clock signal (output, active low to high transition). This signal can be used to trigger an external latch device in receive direction for expansions of the host-port interface.

/HOST_IN_OE:
Host Port In Output Enable signal (output, active low). This signal can be used to enable the output drivers of an external latch device in receive direction for expansions of the host-port interface.

TCLK0, TCLK1:
Timer Clock pins of the TMS320C44 processor. The lines can either be used as outputs to generate external clock signals via the internal timer or they can be switched to inputs in order to count external events or to supply the timers with external clocks. As an alternative, they can be configurated as universal input- and output port-pins.

CLK_3,68MHz:
3.6864 MHz Clock output signal of the SCC2691 board. This clock is stopped when the SCC2691 board is switched to powerdown mode.

H1:
Bus Clock output signal of the TMS320C44 processor. The frequency is half the frequency of the C44CPU board's oscillator.

Connector EE:

The connector EE is a specific C44CPU expansion connector which is not included in the micro-line® standard. The connector EE provides only specific TMS320C44 signals to the outside. These signals are mostly global bus-control signals and C4x communication-port signals.

C2D0...C2D7:
Communication port 2 Data Bus (bidirectional).

/CREQ2:
Communication port 2 token Request (bidirectional).

/CACK2:
Communication port 2 token Request Acknowledge (bidirectional).

/CSTRB2:
Communication port 2 Data Strobe (bidirectional).

/CRDY2:
Communication port 2 Data Ready (bidirectional).

CDIR2:
Communication port 2 Direction (output).

C4D0...C4D7:
Communication port 4 Data Bus (bidirectional).

/CREQ4:
Communication port 4 token Request (bidirectional).

/CACK4:
Communication port 4 token Request Acknowledge (bidirectional).

/CSTRB4:
Communication port 4 Data Strobe (bidirectional).

/CRDY4:
Communication port 4 Data Ready (bidirectional).

CDIR4:
Communication port 4 Direction (output).

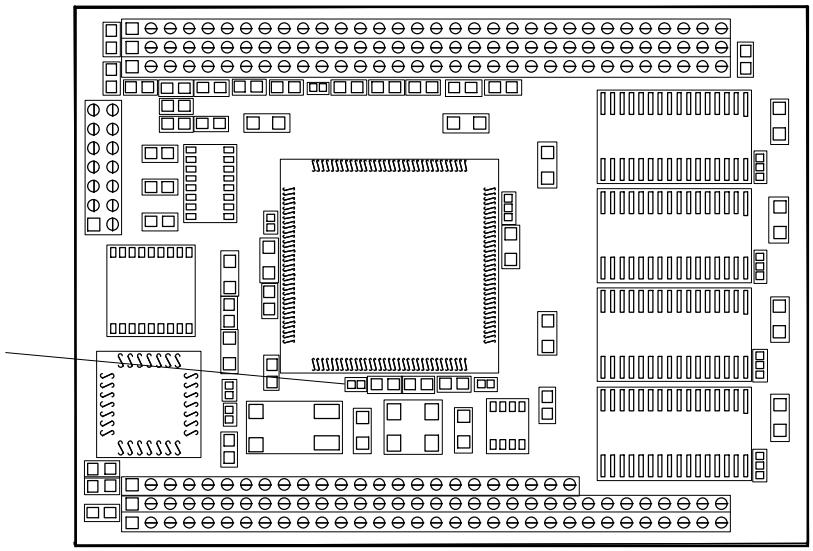
/FLA_CS:
Special pin for ORSYS internal board configurations. This pin is not required for any applications and must remain open.

4.2 Alternative Processor and Boot Modes

4.2.1 Booting via a DSP Link

Instead of the booting via the preset, automatic FILE system user program, the C44CPU board can also be booted via one of the four DSP links. Further information is provided in the TMS320C4x user´s guide. In order to set up DSP-link booting, solder bridge J20 on the C44CPU board has to be open:

activate DSP-link booting
= open solder bridge J20



In order to set up the C44CPU system drive, the first instruction sequence of the loaded program has to be a dummy read access to ´read port 3 / read-write host port register´ (address 0x8023C000[1)]).

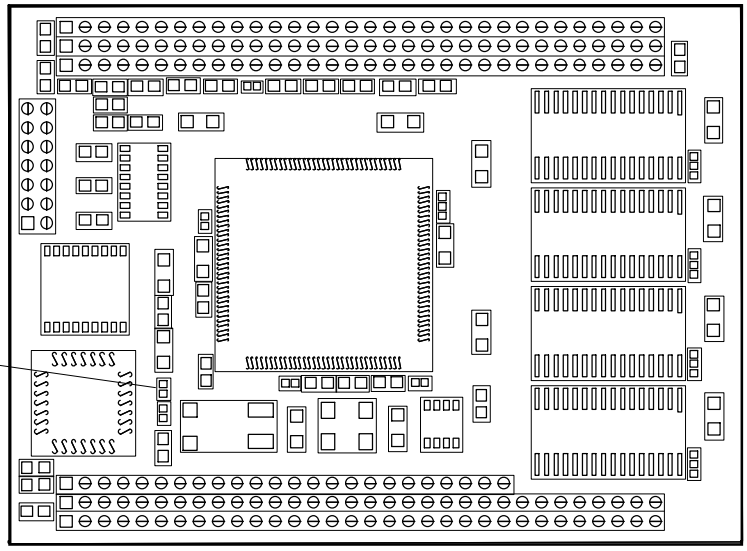
[1)] = addresses are only valid for global memory page = 0 *(= default state after delivery)*

4.2.2 TMS320C44 ROMEN (Rom Enable):

Solder bridge J13 can be closed to deactivate the TMS320C44 internal boot ROM (see TMS320C4x user´s guide, pages 3-18).

TMS320C44 ROMEN = ´0´:
- set solder bridge J13

(default state: ROMEN = ´1´)

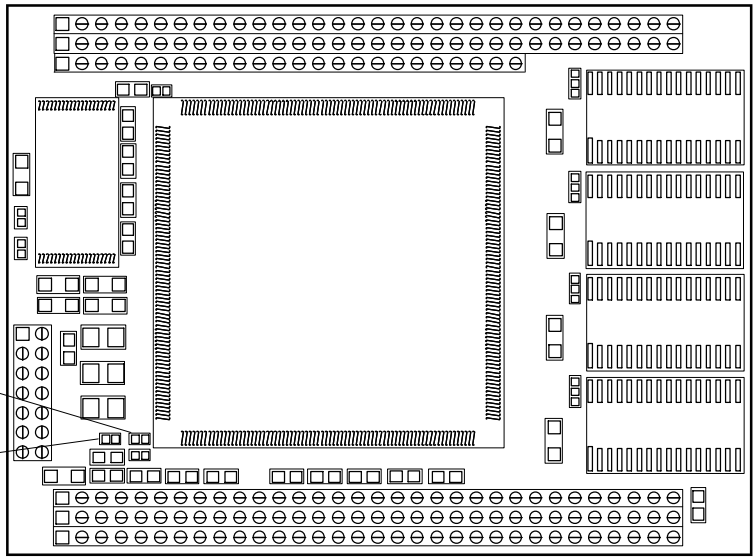


4.2.3 TMS320C44 RESETLOC0, RESETLOC1 (Reset Vector Location):

The TMS320C44 processor has the two signals RESETLOC0 and RESETLOC1 to determine the program start addresses after reset (see TMS320C4x user´s guide, pages 3-17). The value of these signals can be selected by solder bridges J14 and J15.

TMS320C44 RESETLOC1 = ´1´:
- open solder bridge J15

TMS320C44 RESETLOC0 = ´1´:
- open solder bridge J14



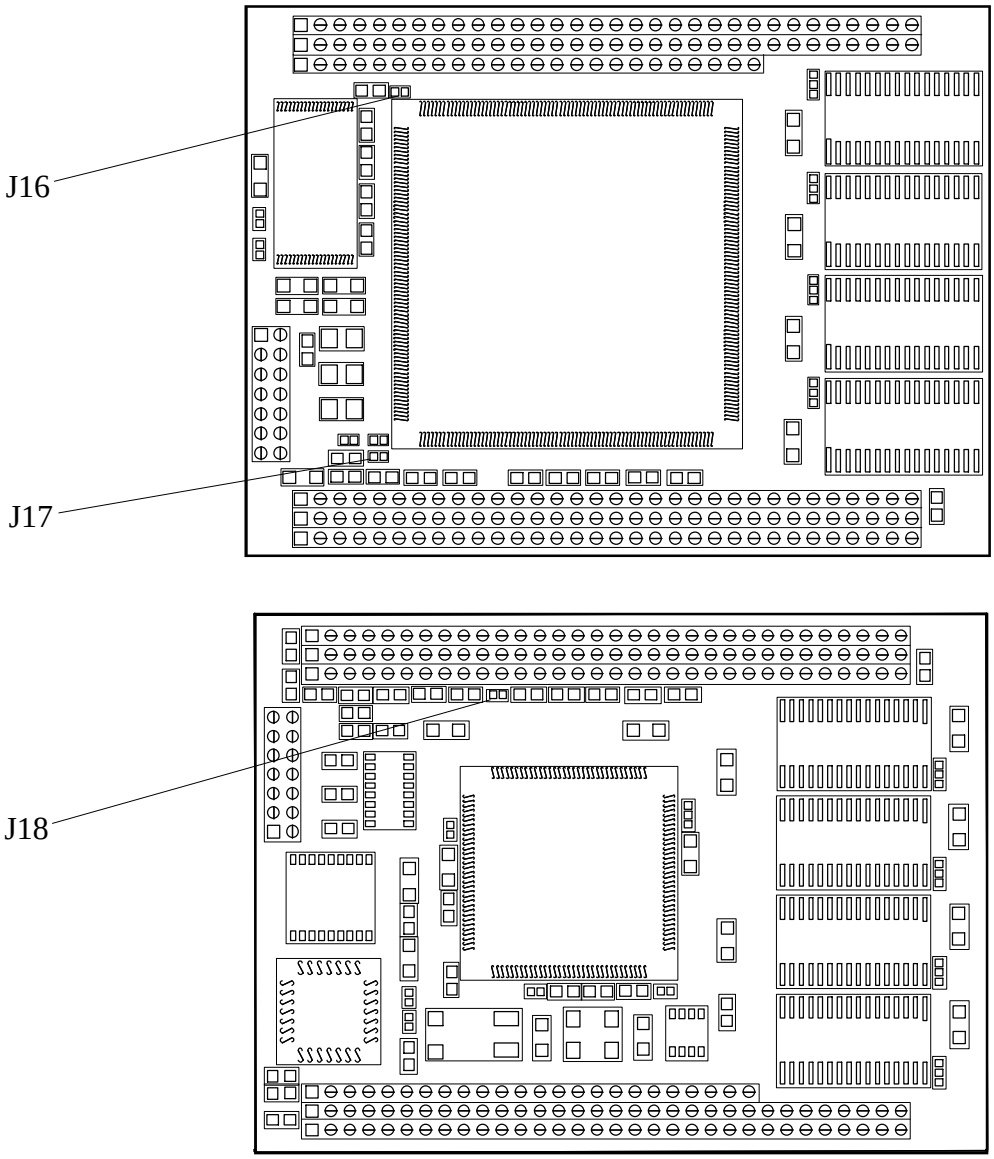
(default state: RESETLOC0 = ´0´, RESETLOC1 = ´0´)

4.3 Setup of the Global Memory Pages 0...7

The C44CPU board has three solder bridges in order to set up the global memory pages 0 to7. There are eight combinations possible:

	page 0	page 1	page 2	page 3	page 4	page 5	page 6	page 7
J18	closed	open	closed	open	closed	open	closed	open
J17	closed	closed	open	open	closed	closed	open	open
J16	closed	closed	closed	closed	open	open	open	open

default state



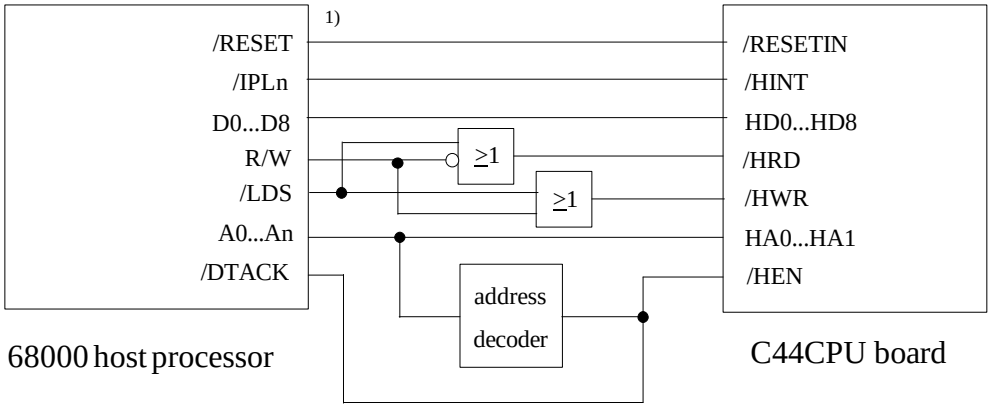
The running application software can find the latest page configuration because a process is activated during the ORSYS firmware booting procedure which tests the hardware page configuration and enters a number from 0 to 7 into the memory address 0x002FFFFF (the highest address of the TMS320C44 processor's internal RAM). This RAM address should not be accessed by the application software.

4.4 Application Examples

4.4.1 Connecting a Parallel Port 82C55 Device via an I/O Port

An application example explains the connecting of a customary peripheral device to the C44CPU board with a 82C55 parallel port device. For the 82C55, the active high RESETOUT signal of the C44CPU board has to be used because the 82C55 reset input signal is also active high. The C44CPU board interrupt inputs /INT0-IIOF0 to /INT3-IIOF3 are not used for the 82C55 because the 82C55 does not have any interrupt outputs.

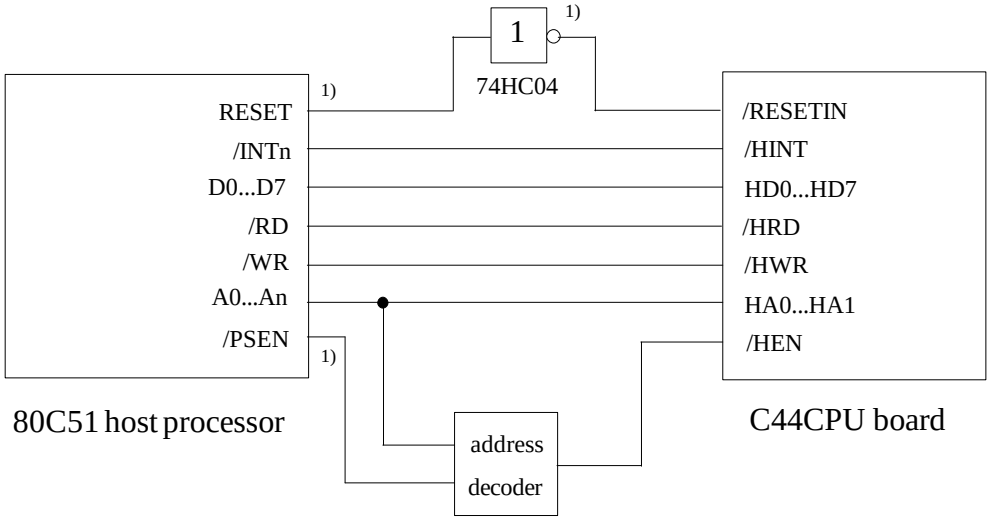
4.4.2 Connecting the C44CPU board as Coprocessor to a MOTOROLA 68000 System via a Parallel Host Port



The above block diagram is an example for connecting the C44CPU board to a MOTOROLA 68000 system. The address decoder selects the I/O base of the four C44CPU host port registers in the 68000 system. The signal pairs R/W (Read /Write) and /LDS (Lower Data Strobe) are connected to the signals /HRD (host read) and /HWR (host write) via two OR logic gates. No further hardware components are necessary.

[1)] = optional

4.4.3 Connecting the C44CPU Board as Coprocessor to an INTEL 80C51 System via the parallel Host Port



In order to connect a C44CPU board to an INTEL 80C51 system, the I/O base of the C44CPU board has to be decoded via an address decoder within the 80C51 system to generate the /HEN signal. The use of the /PSEN signal (Program Strobe Enable) of the 80C51 is optional. The C44CPU board has an independent reset generator, therefore the connection of the inverted RESET signal to the 80C51 system is not mandatorily required.

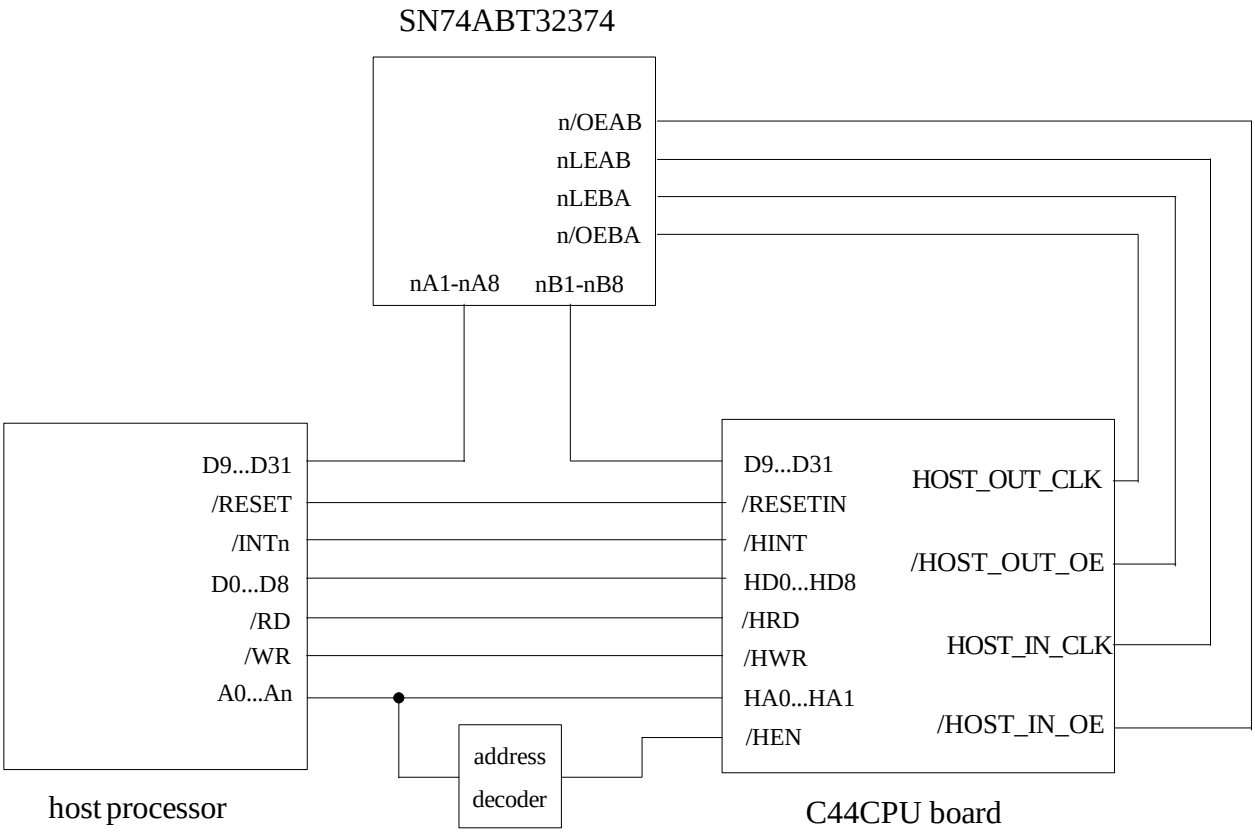
4.4.4 Setup of a DSP-Link Coupled C44CPU Multiprocessor System

The easiest way to set up a DSP-link coupled multiprocessor system is to connect the signal ports of the link ports (see TMS320C4x user´s guide, pages 8-5). There is no need to use CDIRn ports for solutions without external line drivers. **Important:** Without external line drivers, the ground connections between the processor boards must be short and thick!
For multiprocessor solutions, the four DSP-links of each processor can be connected with the links of any other processor.

1) = optional

4.4.5 Extension of the Parallel Host Port to 32 Bits

The extension of the parallel host port to 32 bits enables faster data transfers via the host port because with each transmission cycle, four bytes can be transfered at the same time. The extension can be implemented with an external device together with the C44CPU control signals HOST_OUT_CLK, /HOST_OUT_OE, HOST_IN_CLK and /HOST_IN_OE. The external board is a bidirectional 32-bit latch buffer SN74ABT32374 from Texas Instruments including four bidirectional74374 latch buffers. A 17-bit or a 25-bit extension is possible when correspondingly smaller latches are used.

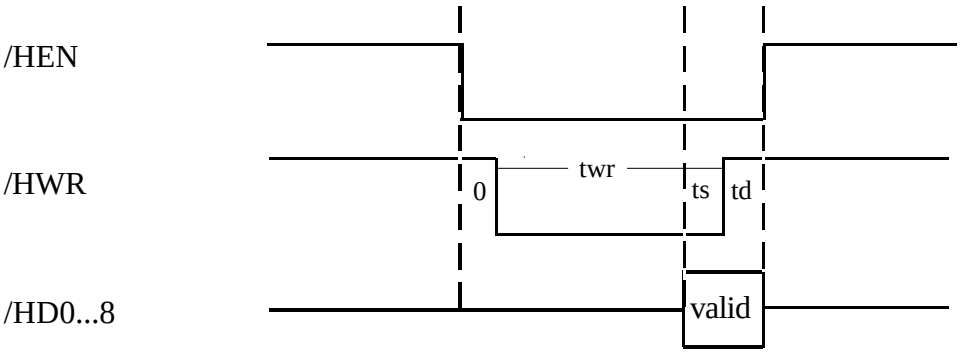


4.5 Further Remarks

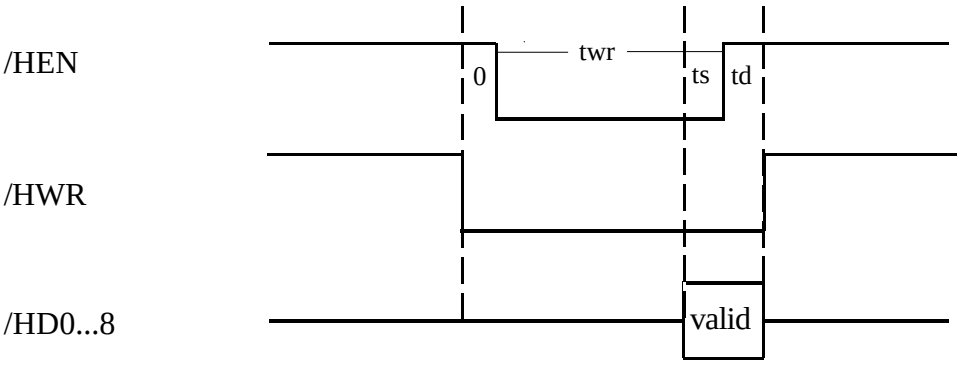
4.5.1 Host-Port Timing

The following timing parameters are important when connecting an external processor to the C44CPU host port:

Host Write access,
/HWR controlled:

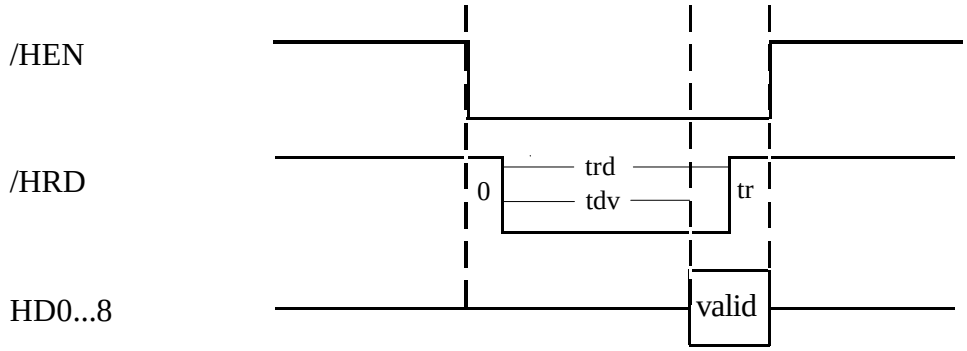


Host Write access,
/HEN controlled:

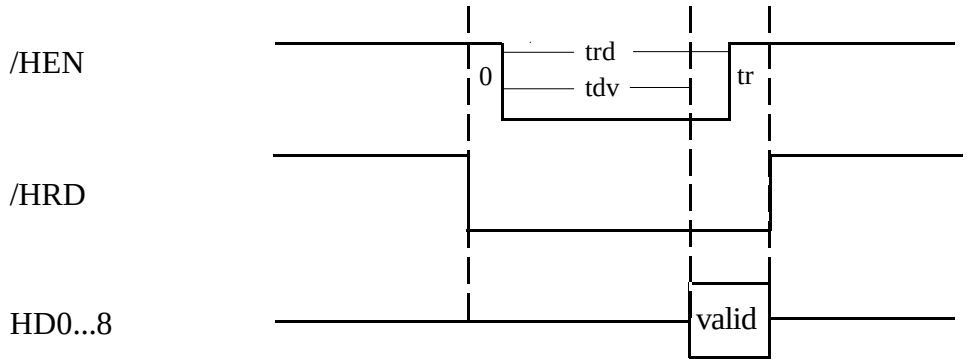


FPGA device	EPX780-10	EPX780-15
twr (write cycle time)	min. 16 ns	min. 21 ns
ts (data setup time)	min. 4 ns	min. 6 ns
td (data hold time)	min. 6 ns	min. 9 ns

Host Read access,
/HRD controlled:



Host Read access,
/HEN controlled:



FPGA device	EPX780-10	EPX780-15
trd (read cycle time)	min. 23 ns	min. 34 ns
tdv (data valid time)	min. 20 ns	min. 30 ns
tr (data release time)	min. 20 ns	min. 30 ns

4.5.2 Important Notes to External Hardware Configurations

Due to the C44CPU board's high clock frequencies and fast transients the following rules always have to be observed when connecting external hardware components to the C44CPU board:

- Bus lines as well as fast control lines should not be longer than 15 cm, otherwise the signals on the critical lines need to be measured during C44CPU board operation and if necessary, impedances of the lines have to be adapted by serial resistors.
- the external ground and power supply should be realized as copper planes. The tracks between the power supply, ground planes and peripheral devices have to be short, thick and be decoupled by a support capacitor of about 100 nF (to +5V) ! In case of experimental bread boards, all ground- and +5V wires should be at least 1.5 mm^2 thick. The basic rule is the thicker, the better.
- For connections of noise-sensitive AD- or DA converters, the analog and the digital ground configurations have to comply with the instructions of the converter data sheet.

4.5.3 Signal Loads

The following guidelines apply to all fast processor signals (D0...D31, A0...A23, R/W_n, /STRB_n, /RD_0, /WR_0, STAT0...3, PAGE_n and H1):

- signal loads are usually about 80 pF
- signal loads above 160 pF should be avoided

All other C44CPU board signals should be below 200 pF.

4.5.4 Ambient Temperature

Storage temperature: -25...+85^{0}C
Opertion temperature: 0...70^{0}C

4.5.5 Power Consumption

The actual C44CPU board power consumption mostly depends on the number of external RAM accesses. The power consumption can be reduced by activating the powerdown modes of the SCC2691 device (see SCC2691 data sheet) and of the RS232 driver (C44CPU control register). The TMS320C44 processor supports a powerdown mode which stops the processor. The processor is reactivated by an external interrupt signal (see TMS320C44 user 's guide). The powerdown mode is generally used for a power reduction during pauses between the sequence of data bursts.

clock frequency	TMS320C44 idle-mode[1)]	only internal memory accesses[2)]	all memory accesses external: 32K words 0 WS RAM [2) 3) 4)]
40 MHz	about 40 mA	about 440 mA	about 830 mA
50 MHz	about 45 mA	about 470 mA	about 860 mA
60 MHz	about 50 mA	about 500 mA	about 890 mA
80 MHz	about 55 mA	about 530 mA	about 920 mA

[1)] = processor clock = 0 (idle mode); SCC2691 and RS232 drivers in the powerdown mode; local RAM bank inactive

[2)] = maximum system speed; SCC2691 and RS232 driver active

[3)] = an additional power consumption of about 15 % has to be considered for the 128K-word RAM.

[4)] = TMS320C44 cache memory inactive; program and data are in the external local and global RAM memory of the C44CPU board.

4.5.6 C44CPU Board Dimensions

All dimensions are provided in mm.